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AAP11/AAP21

Schematic Document

SKL-H paltform with Nvidia N16E-GS/GT/GX

Rev: 1.0(A00) PVT

2015/07/21

@ : Nopop Component

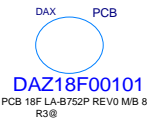
EMI@ /@EMI@ : EMI pop/unpop part
ESD@ /@ESD@ : ESD pop/unpop part
RF@ /@RF@ : RF pop/unpop part

CONN@ : Connector Component

AOAC@ : Intel AOAC
DS3/NODS3: deepS3
TBT@: ThunderBolt
PD@: Power Delivery

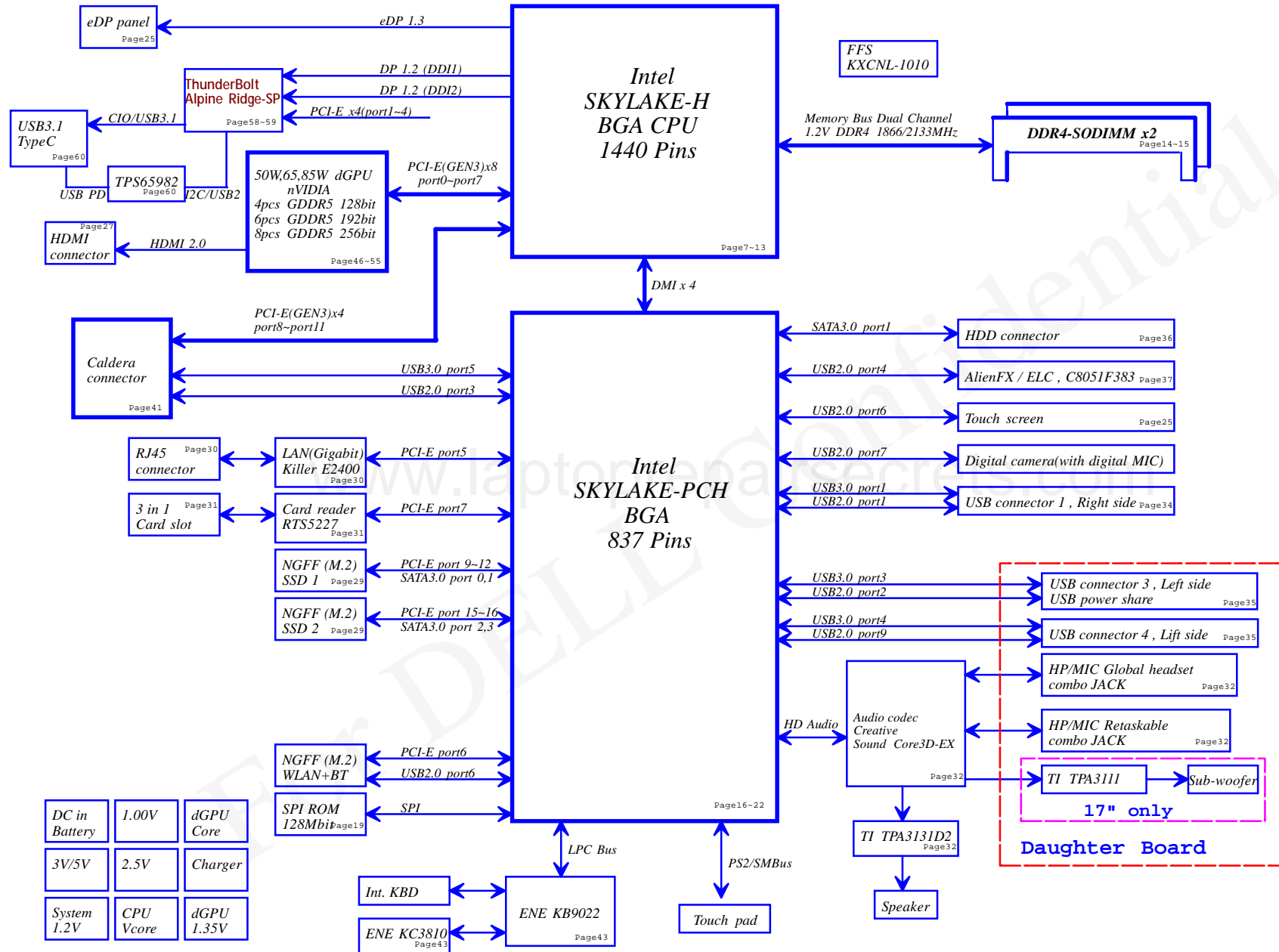
DIS@ : Discrete Part

N16EGS@:N16E-GS(2G)
N16EGT@:N16E-GT(3G)
N16EGX@:N16E-GX(4G)
2G@:2G VRAM
3G@:3G VRAM
4G@:4G VRAM



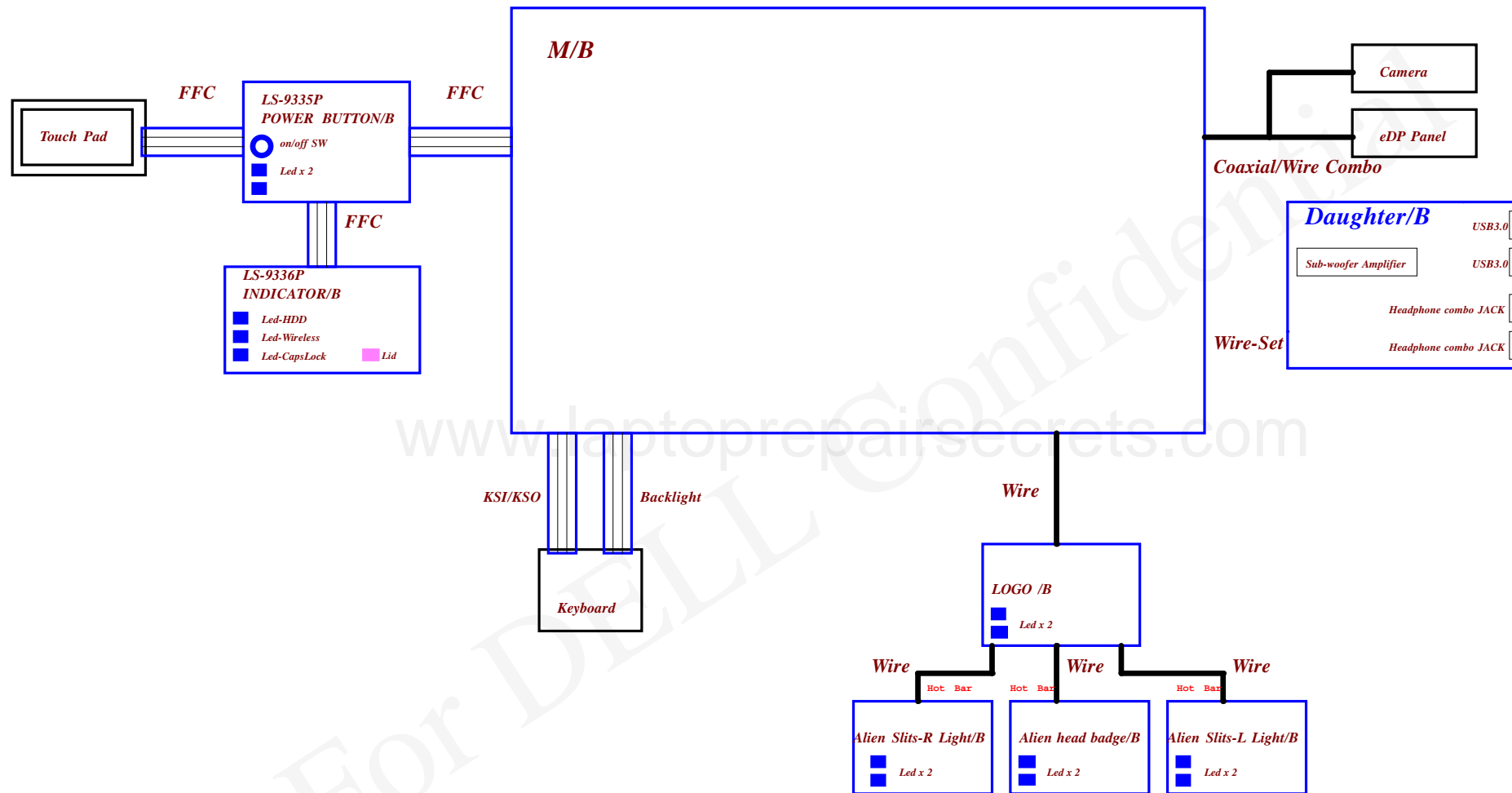
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Size		Document Number		Rev	
Custom		LA-C912P		0.1	
Date:		Wednesday, July 22, 2015		Sheet 1 of 78	

SKL+NV Block Diagram



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				Rev	0.1
				Date	Wednesday, July 22, 2015
				Sheet	2 of 78

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				Size	Document Number
				Date:	Wednesday, July 22, 2015
				Sheet	3 of 78
				Rev	0.1

Board ID Table for AD channel

Vcc	3.3V +/- 1%					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	NVIDIA Graphic
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	AMD Graphic
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF	

Board ID TABLE

ID	PCB Revision
NV	AMD
0	10
1	11
2	12
3	13
4	14
5	15

TBT connector change to SMD type.

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N16)
CLKOUT_PCIE5	DGPU (Caldera)

Symbol Note :



: means Digital Ground



: means Analog Ground

USB3.0

Port1	Right side1
Port2	Right side2
Port3	Left side 1
Port4	
Port5	Caldera
Port6	Left side 2

USB2.0

Port0	Right side1
Port1	Left side 1 (PowerShare)
Port2	Caldera
Port3	ELC
Port4	BT
Port5	Touch screen
Port6	Camera
Port7 / 8	Right side 2 Left side 2

PCI EXPRESS

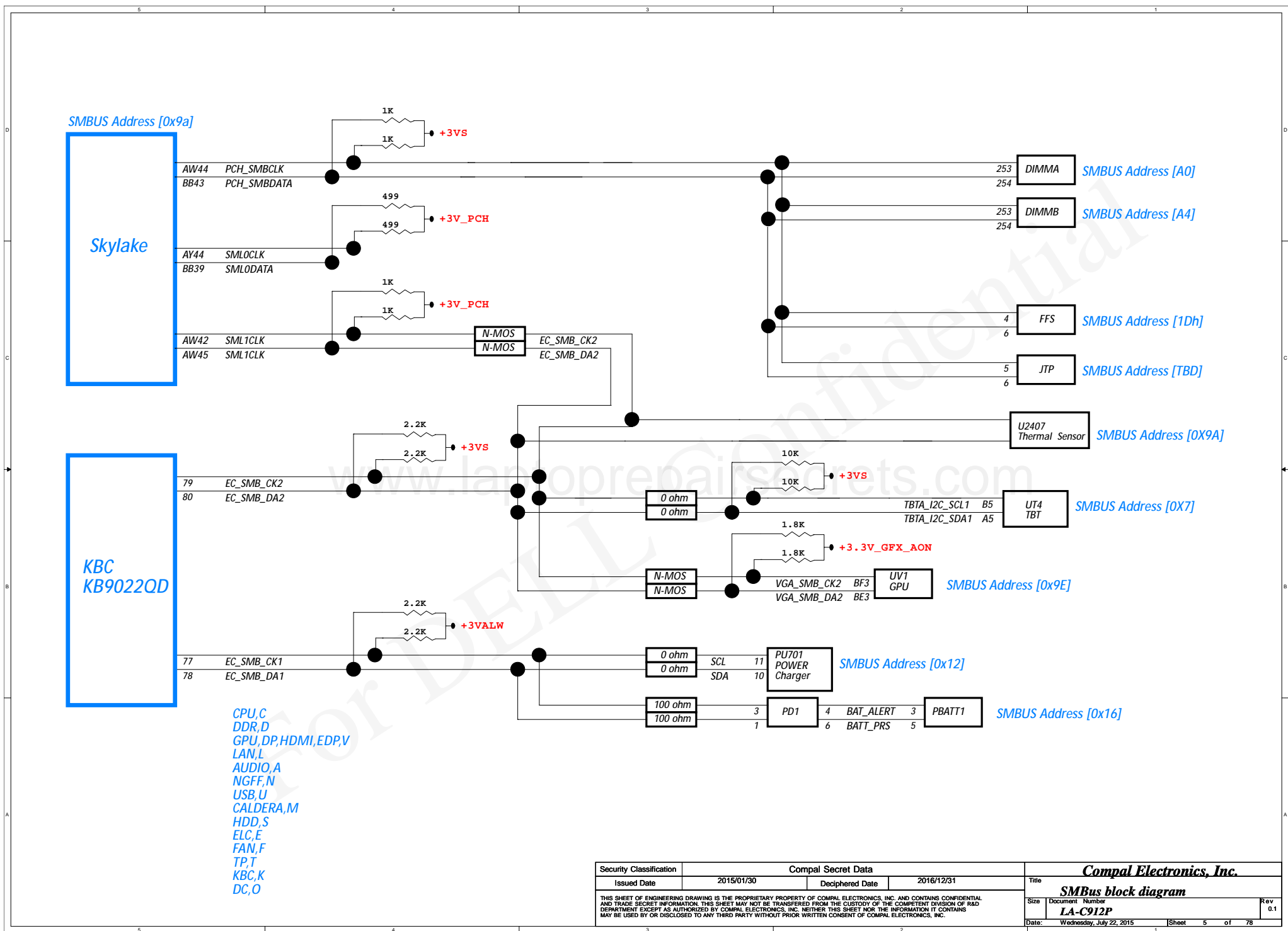
Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	M.2 Card WLAN
Lane 5	PCIE 4x MUX
Lane 6	

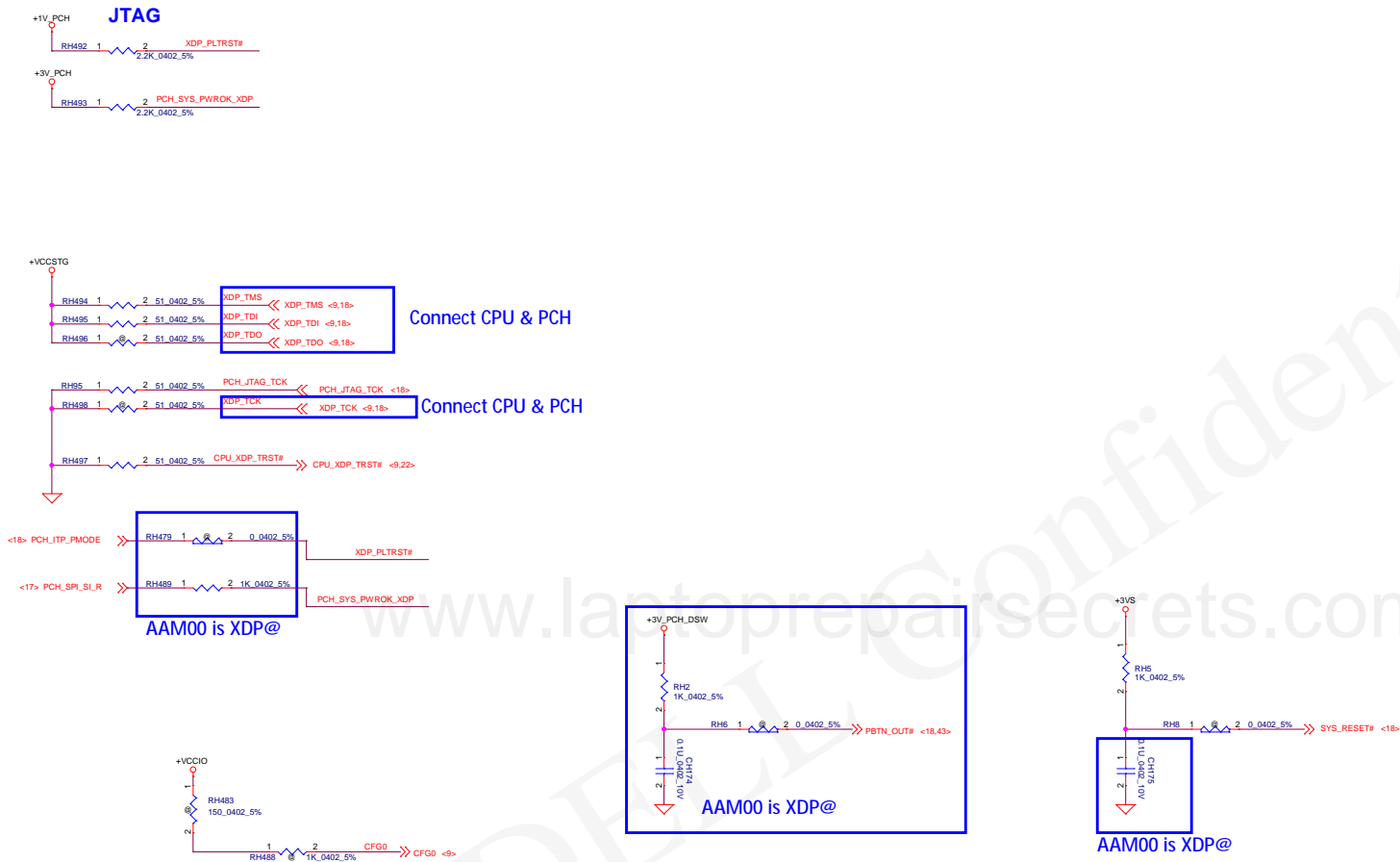
SATA

SATA0	HDD
SATA1	NGFF SSD
SATA2	NGFF SSD
SATA3	

BDW

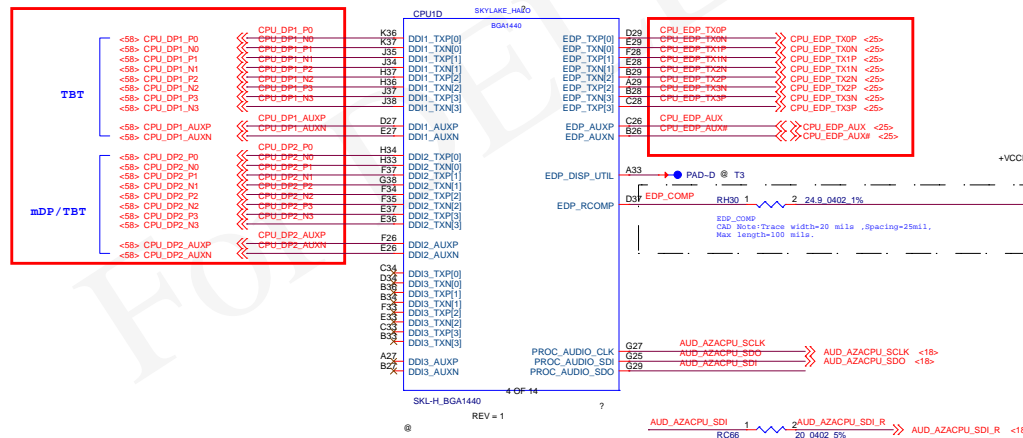
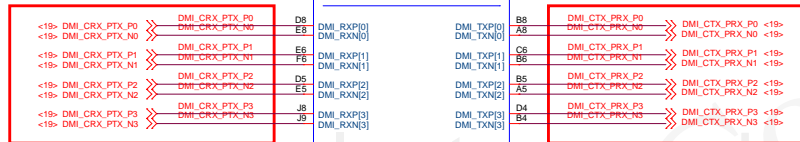
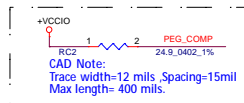
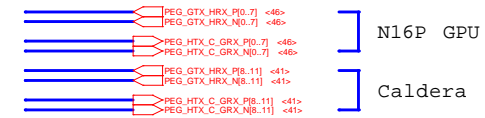
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					LA-C912P	0.1
				Date	Wednesday, July 22, 2015	Sheet 4 of 78





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Size	Document Number	Rev	0.1	
Date:	Wednesday, July 22, 2015	Sheet	6	of 78

PEG Lane Reversed

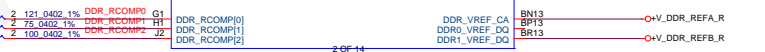
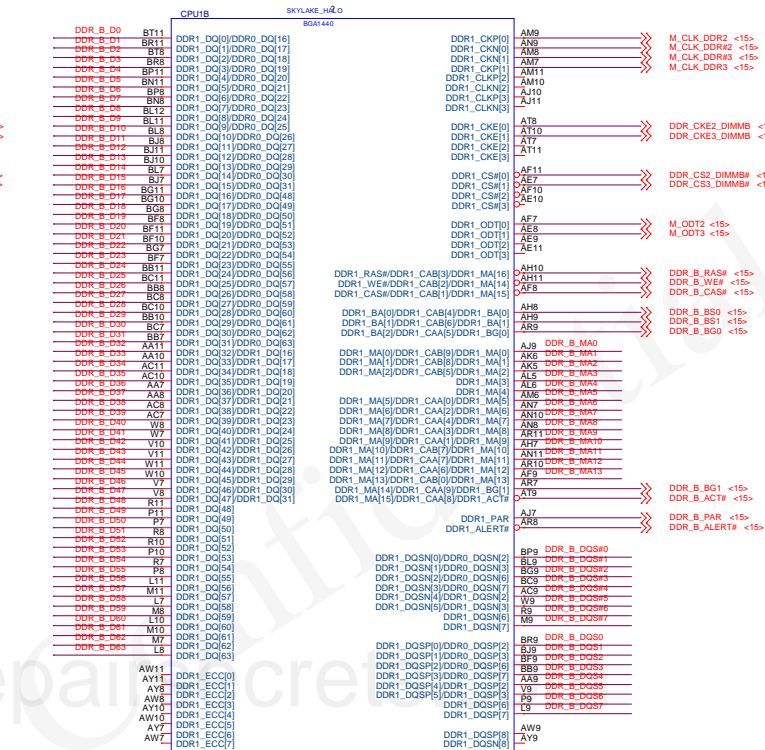
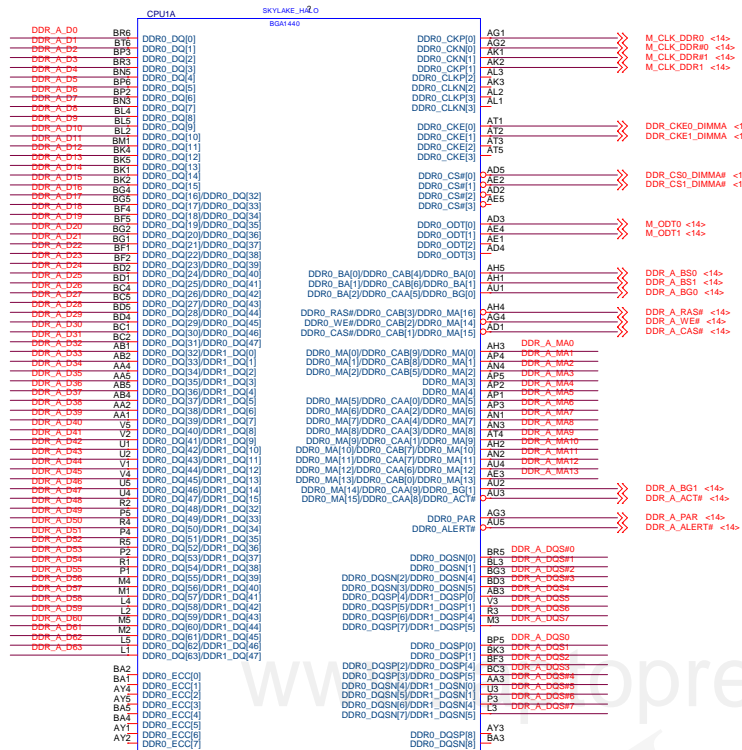


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				Date	Wednesday, July 22, 2015
				Sheet	7 of 78
				Rev	0.1

Interleave

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 <14> DDR_A.MA[0..13]
 <14> DDR_A.DQS[0..7]
 <14> DDR_A.DQS[0..7]

<15> DDR_B.DQ[0..63]
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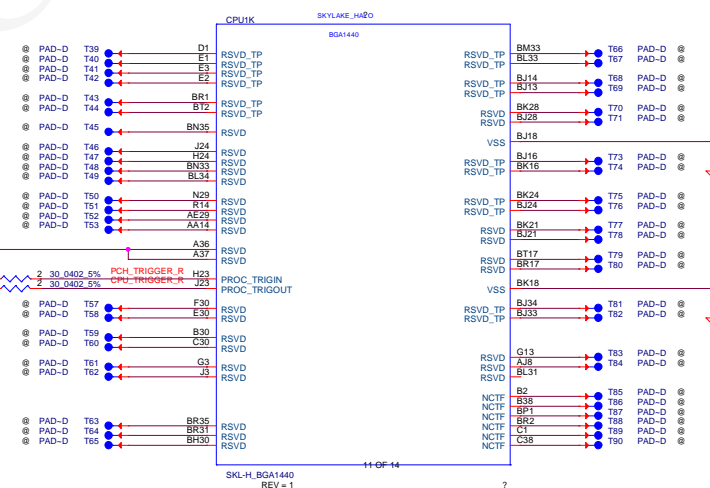
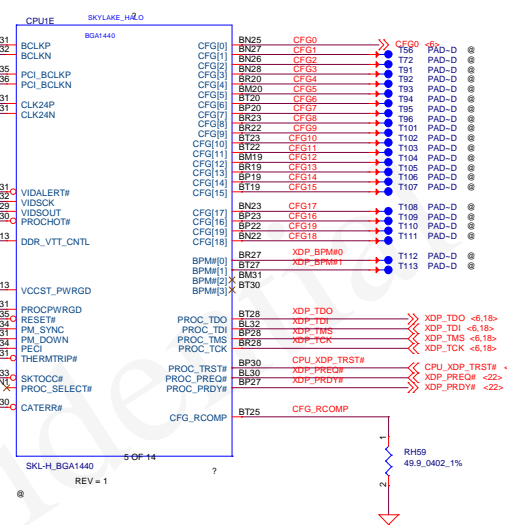
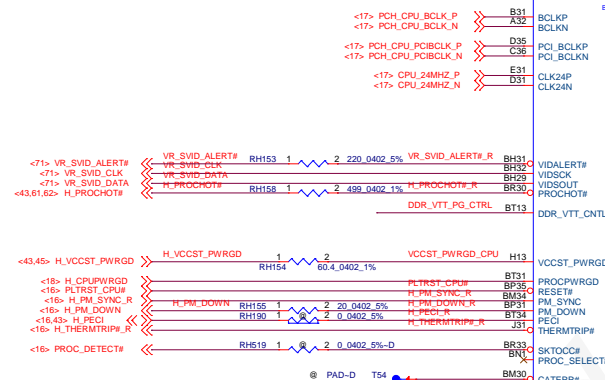
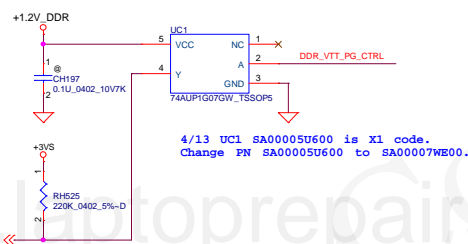
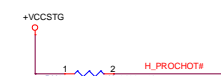
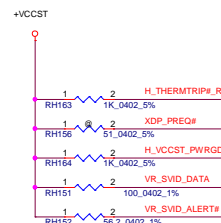
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				Document Number	0.1
				Date: Wednesday, July 22, 2015	Sheet 8 of 78

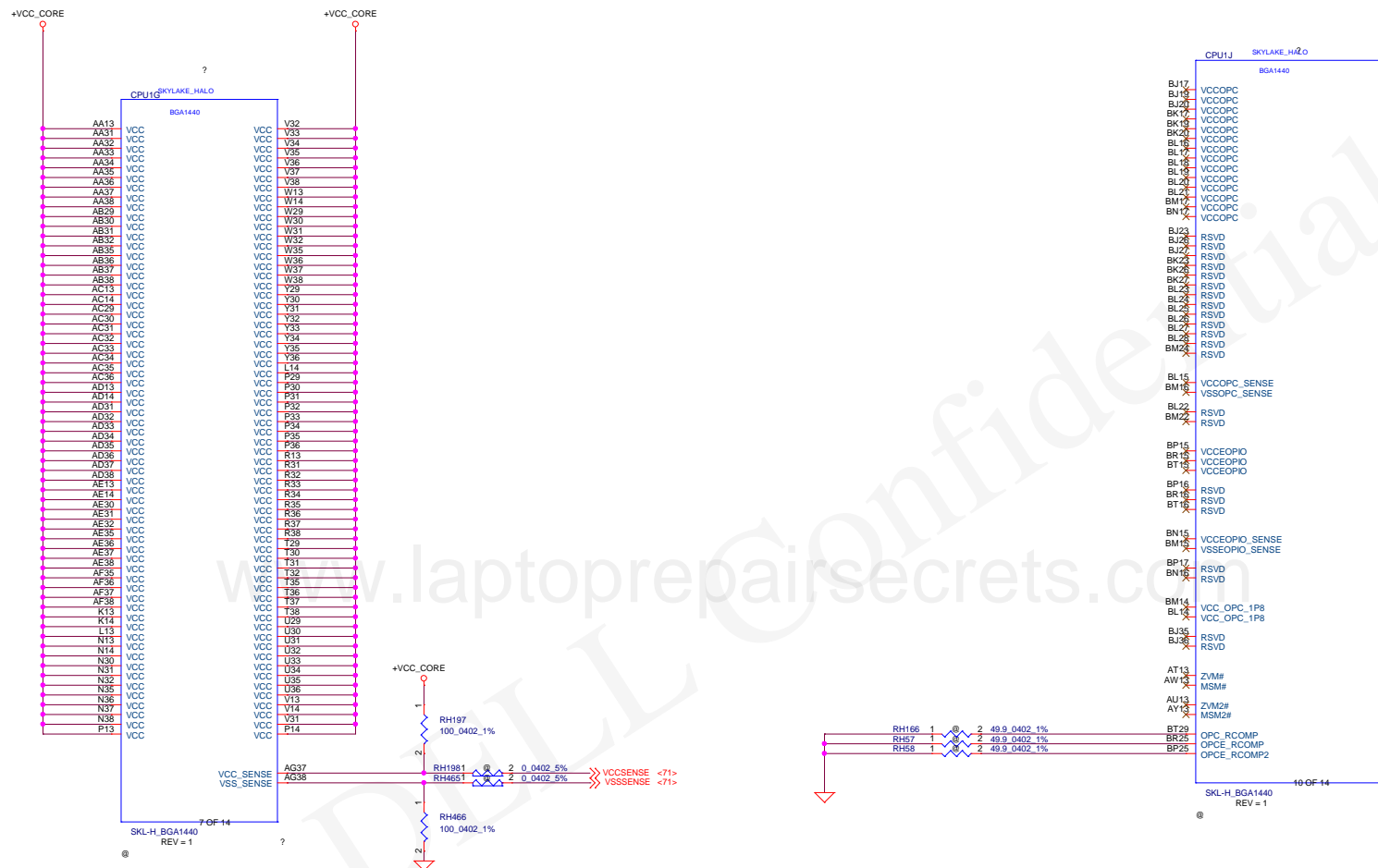
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1 RH188

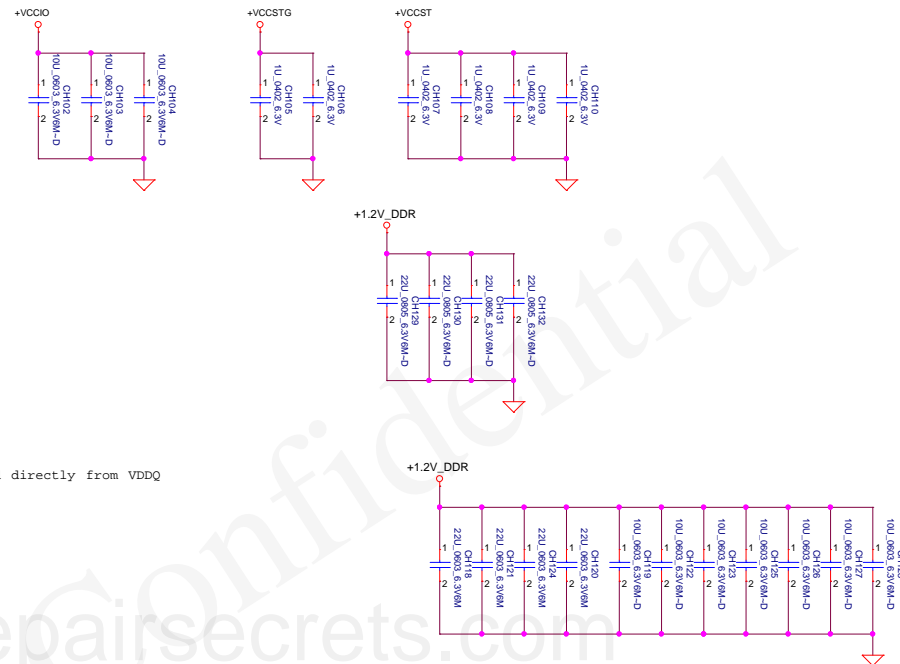
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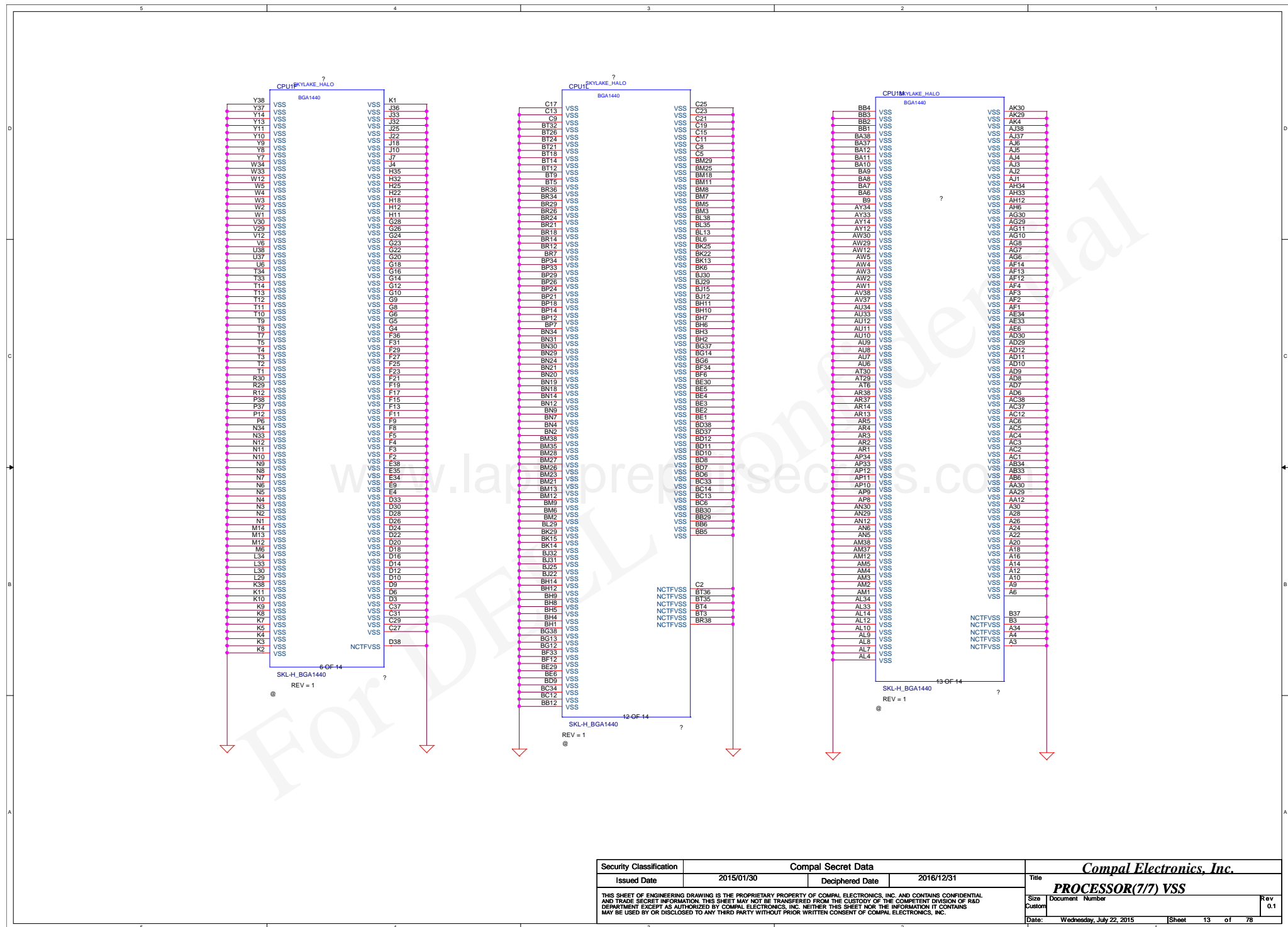
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				Sheet	10 of 78
				Rev	0.1

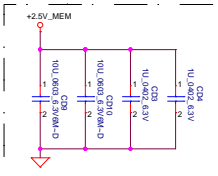


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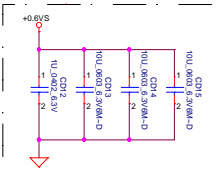


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Date:				Wednesday, July 22, 2015		Sheet 13 of 78	

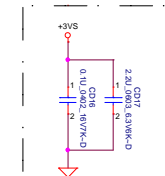
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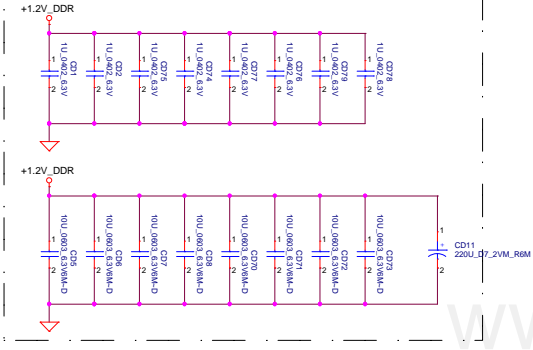
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Layout Note:
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Layout Note:
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<< DDR_A_BG0 >>

<< DDR_A_MA12 >>

<< DDR_A_MA11 >>

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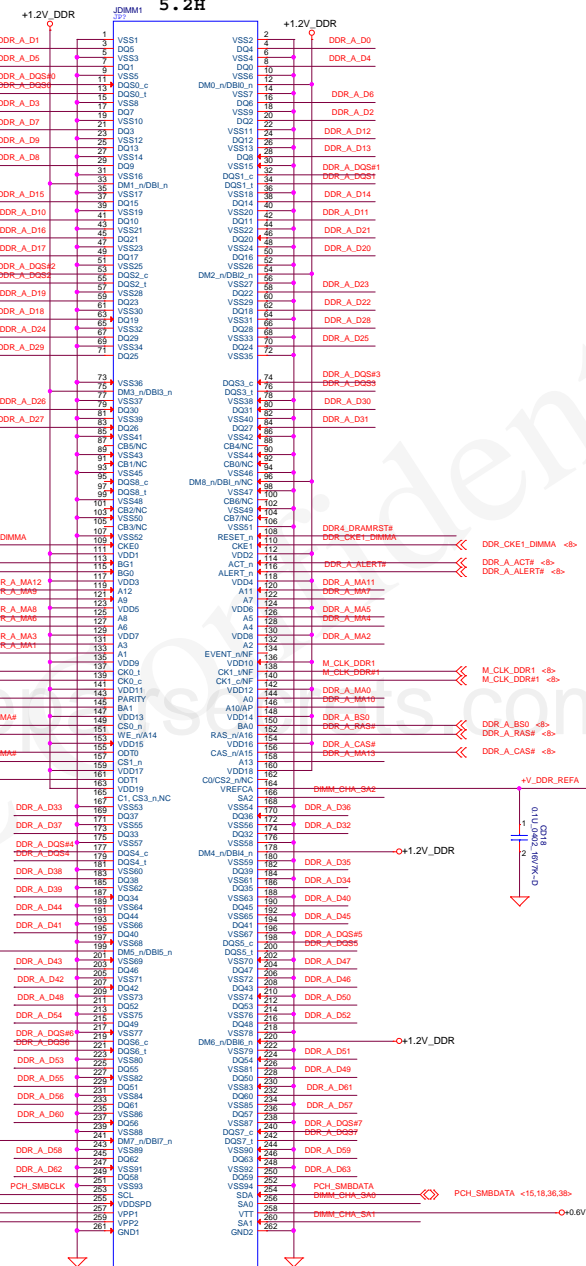
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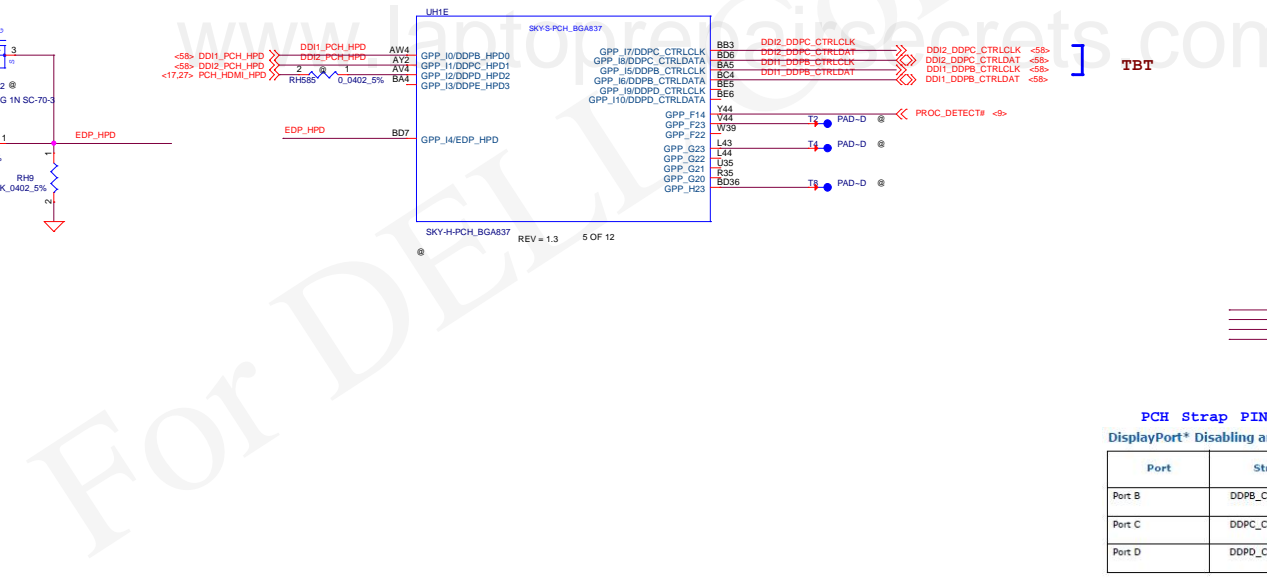
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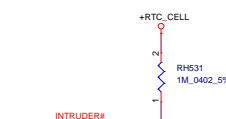
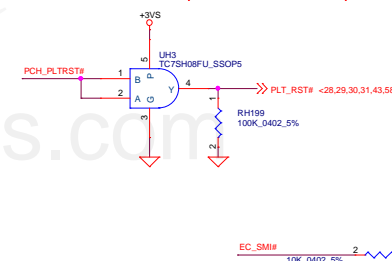
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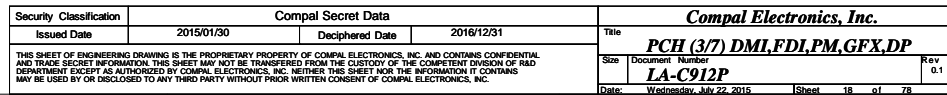
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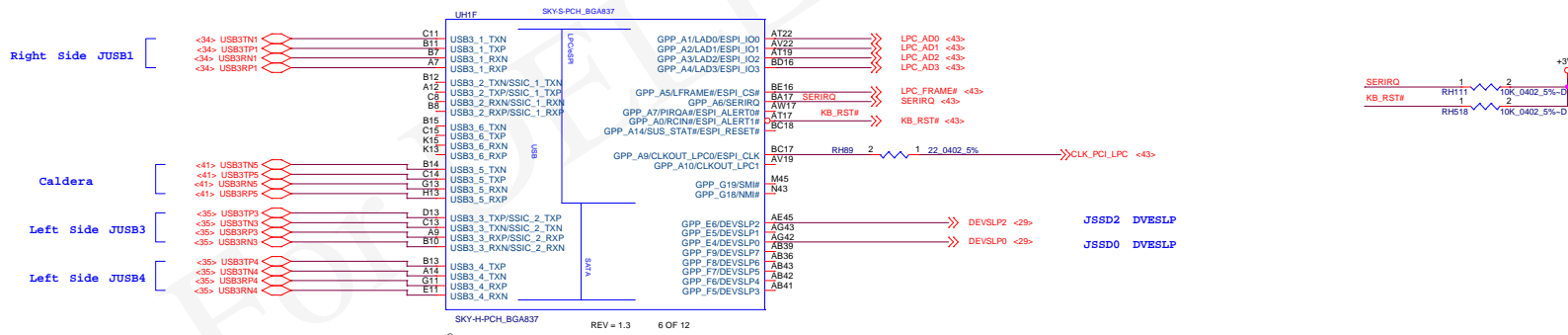
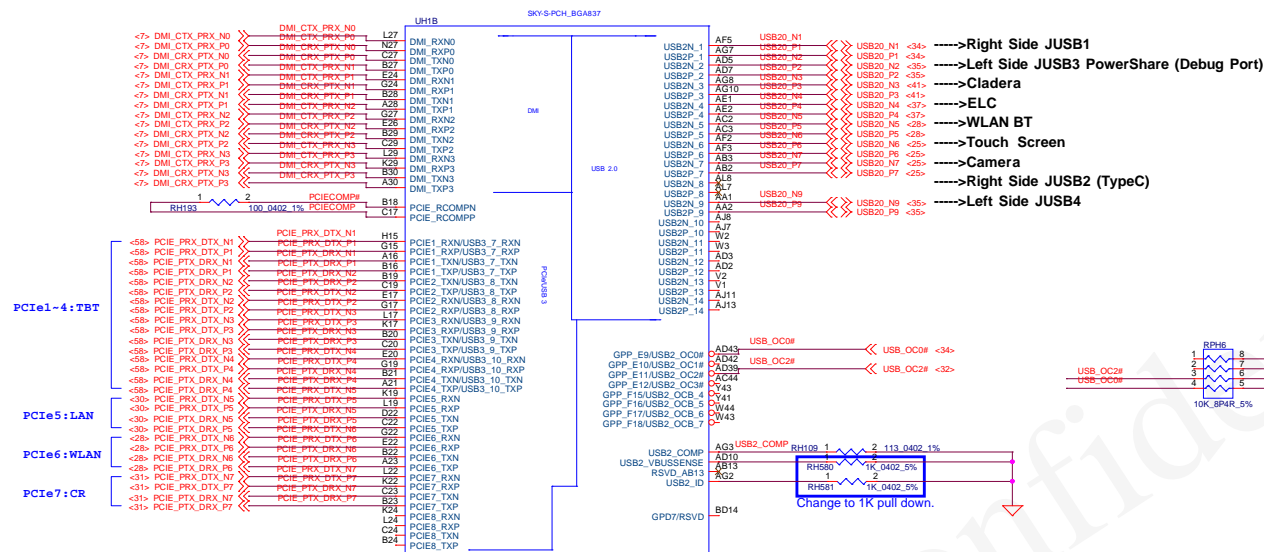
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				Date	Wednesday, July 22, 2015
				Sheet	14 of 78



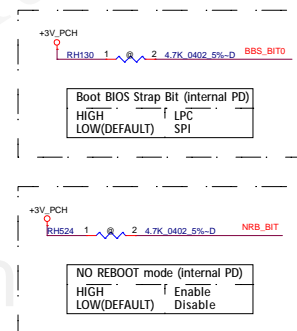
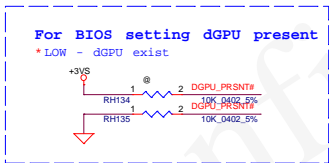
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HDA_SYNC Isolation Circuit

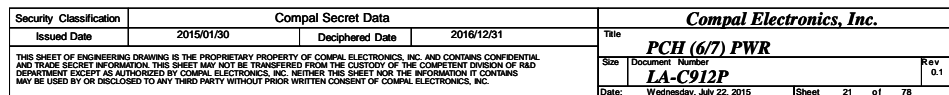




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Size	Document Number	Date	Wedsessday, July 22, 2015	Sheet	19 of 78



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Date:				Wednesday, Jul 22, 2015	Sheet 20 of 78



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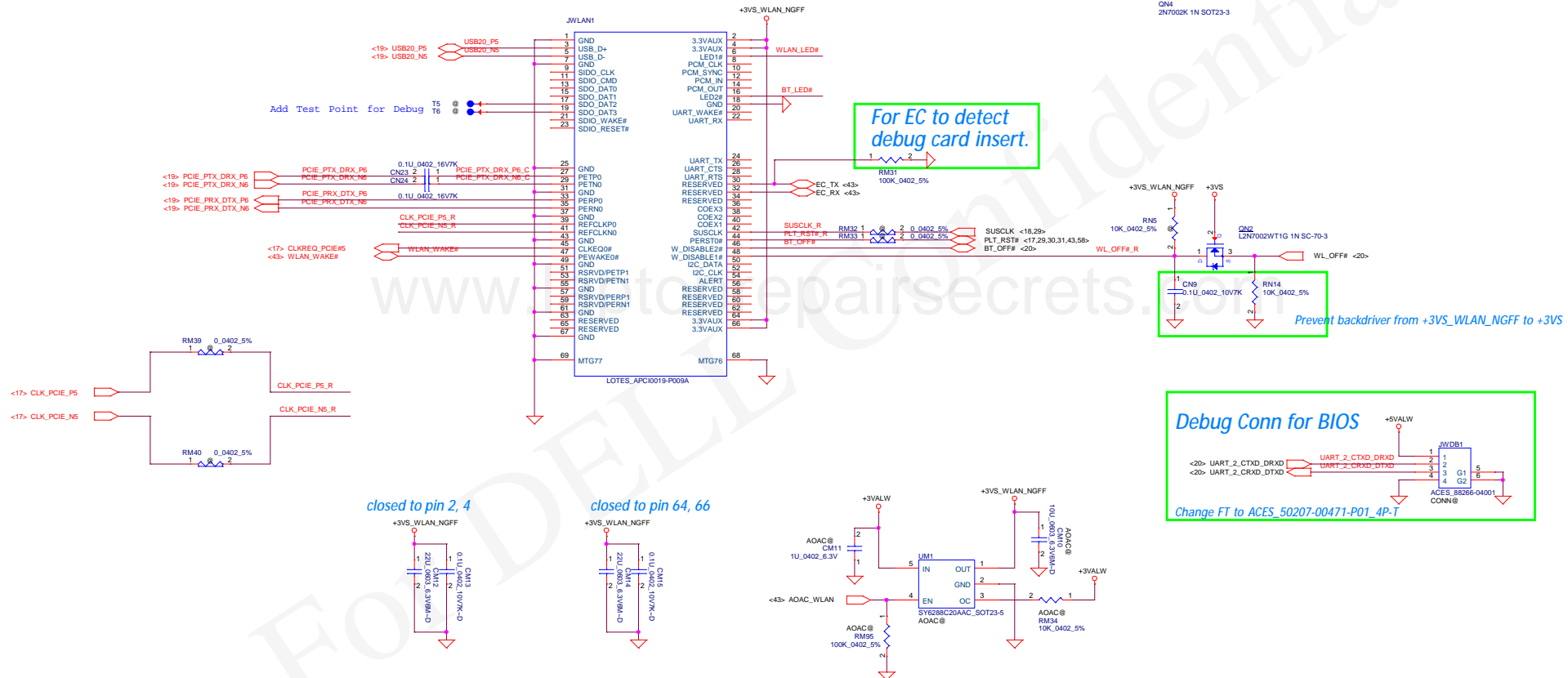
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				LA-C912P	
Date: Wednesday, July 22, 2015				Sheet	24 of 78
				Rev	0.1

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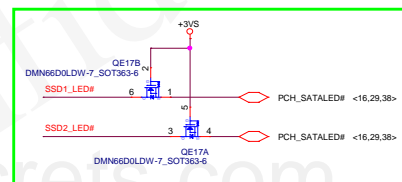
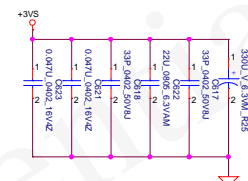
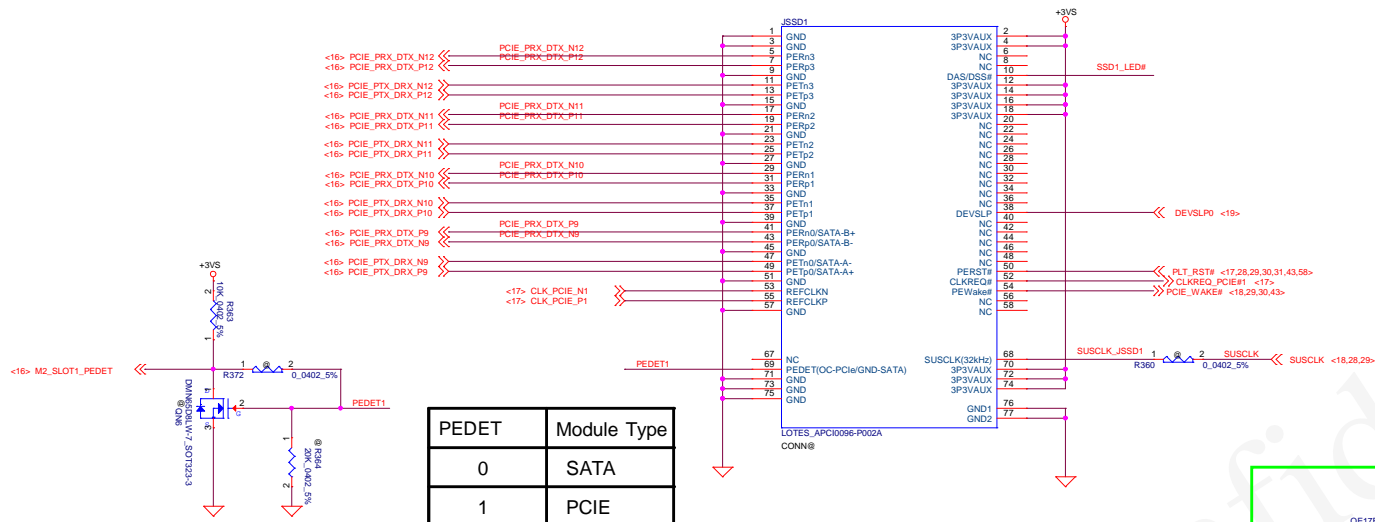
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				Size	Document Number	Rev
				Custom	LA-C912P	0.1
Date: Wednesday, July 22, 2015				Sheet	26 of 78	

NGFF WL Con (Key E)

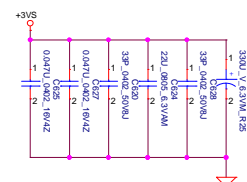
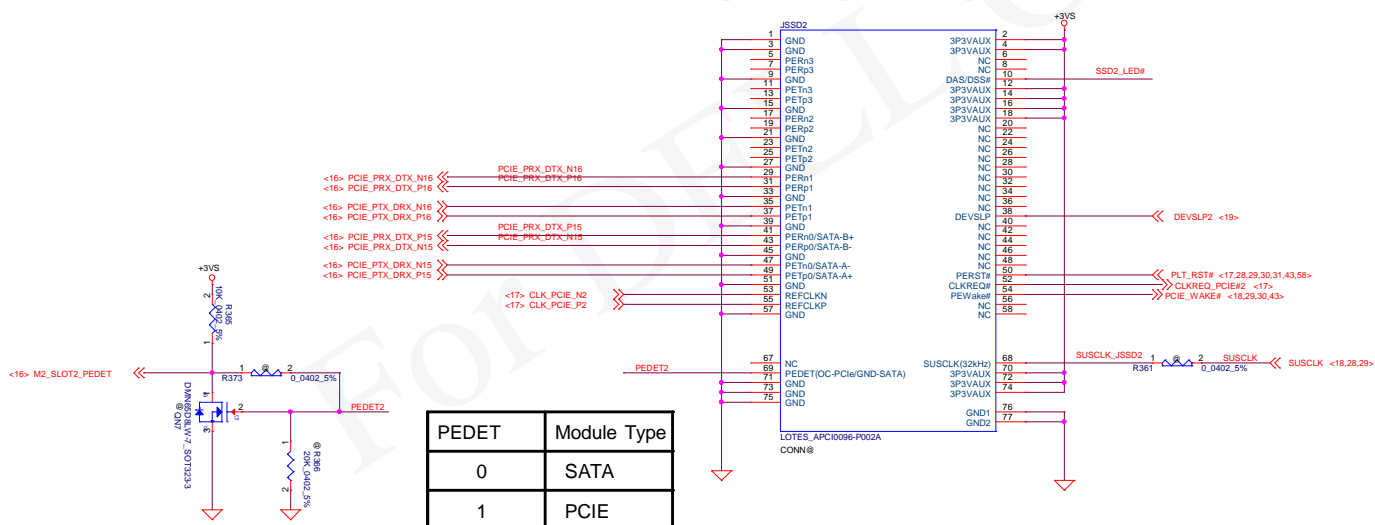


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				Document Number
				LA-C912P
				Rev
				0.1
				Date
				Wednesday, July 22, 2015
				Sheet
				28 of 78

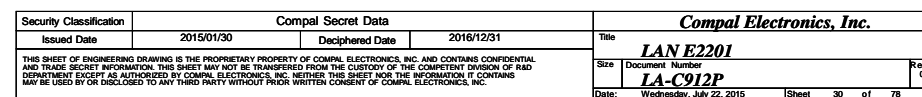
SSD NGFF slot_1 Key M

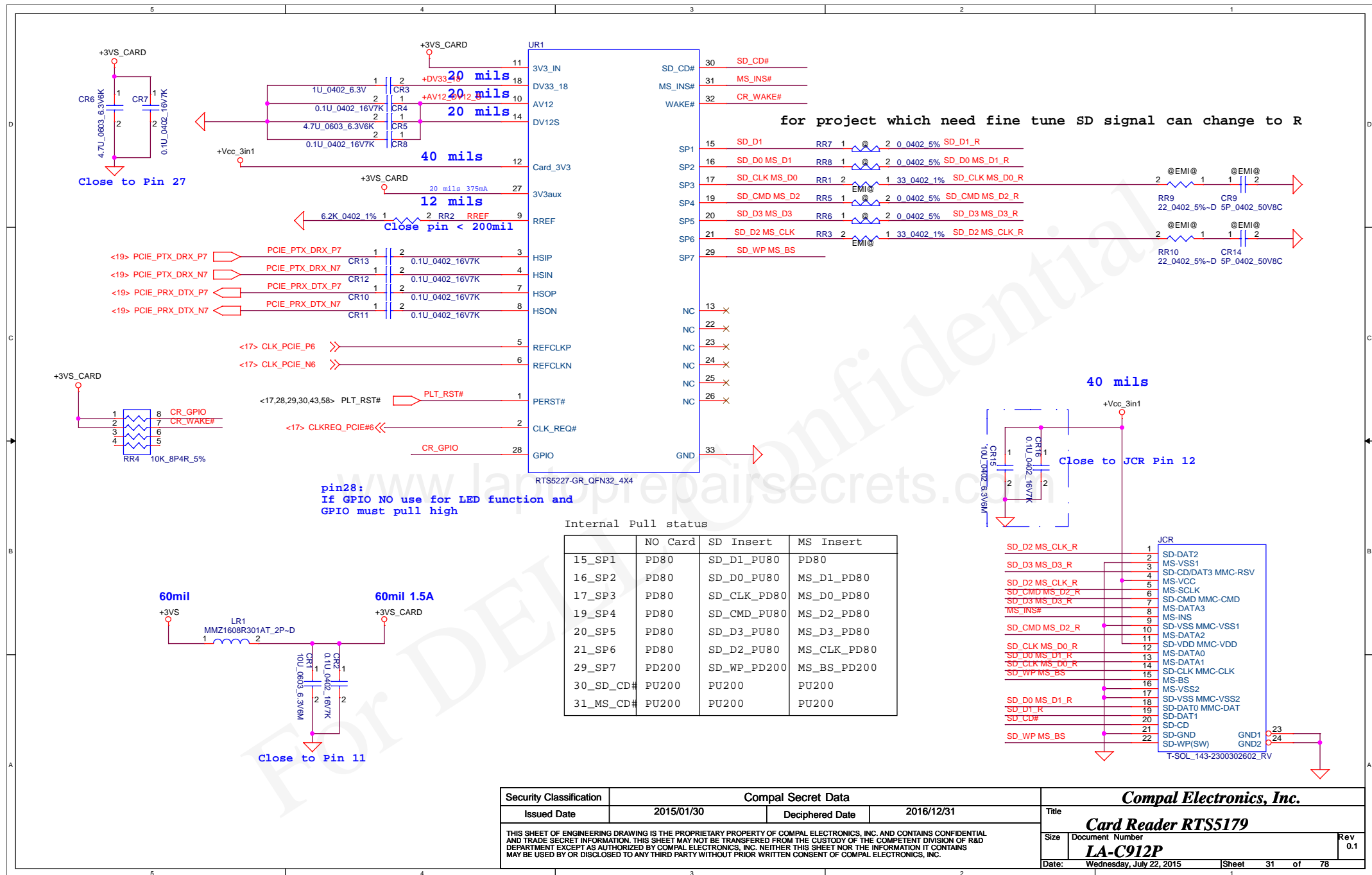


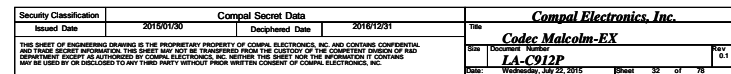
SSD NGFF slot_2 Key M



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					LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	29 of 78
				Rev	0.1



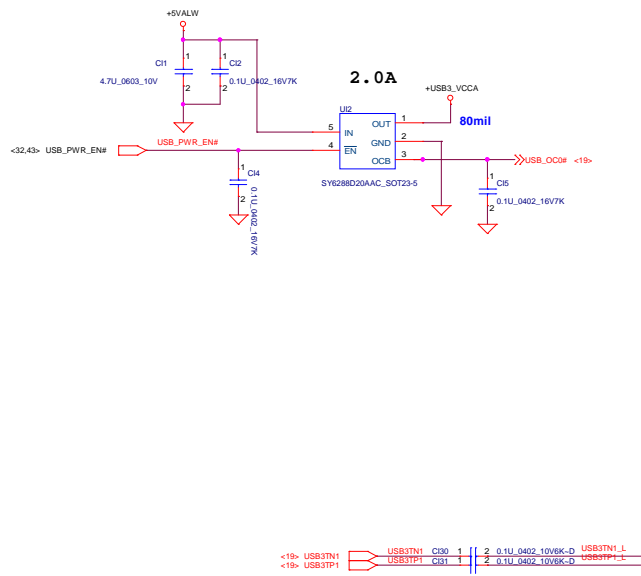




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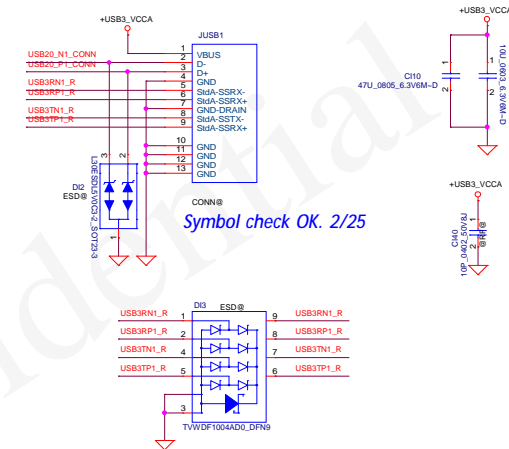
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				Date	Wednesday, July 22, 2015



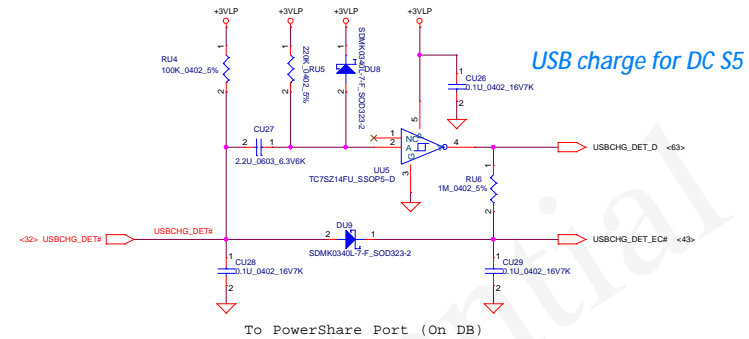
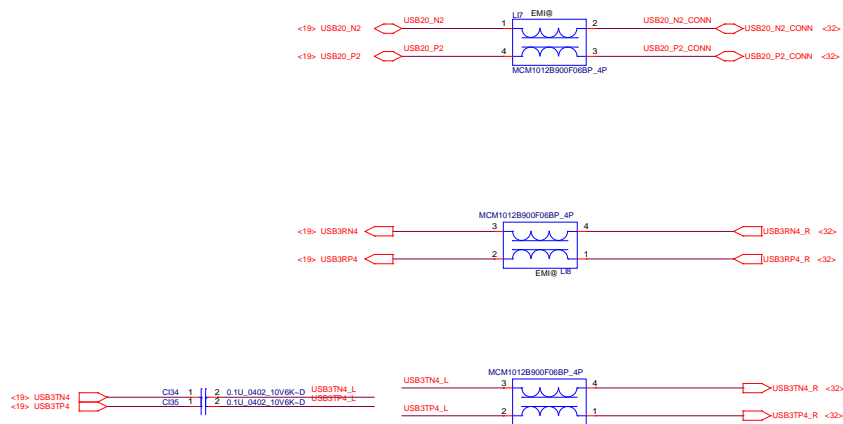
JUSB1

On MB (Right Side)

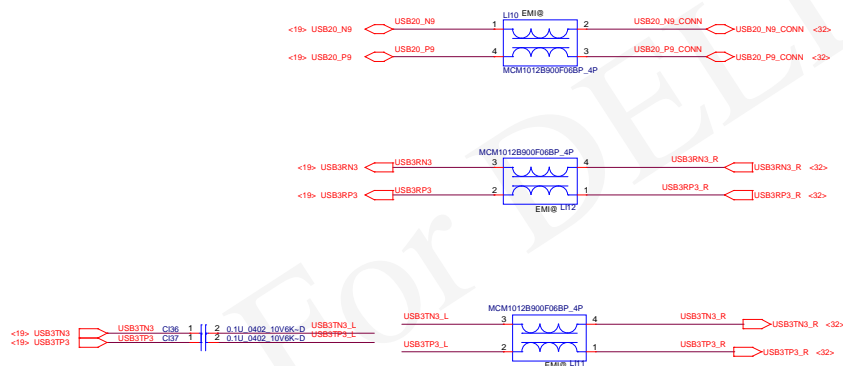


JUSB2 change to TypeC

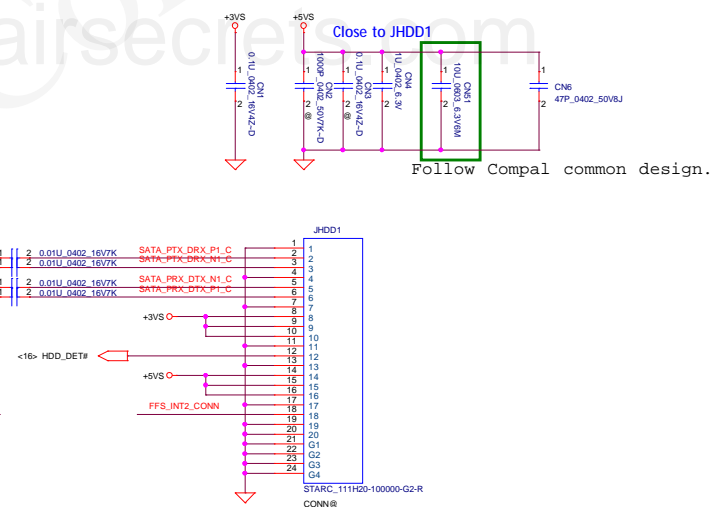
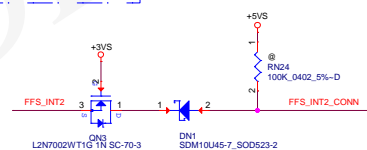
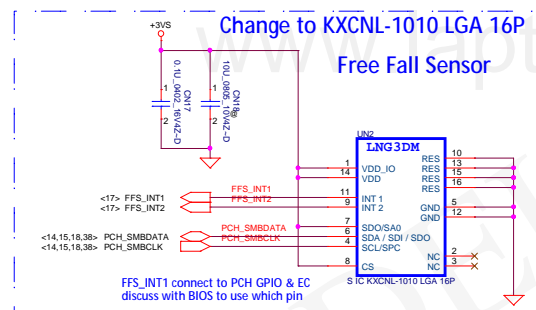
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Compal Electronics, Inc.				Size Document Number
USB 3.0/2.0 x2 (left side)				LA-C912P
Date: Wednesday, July 22, 2015				1Sheet 34 of 76



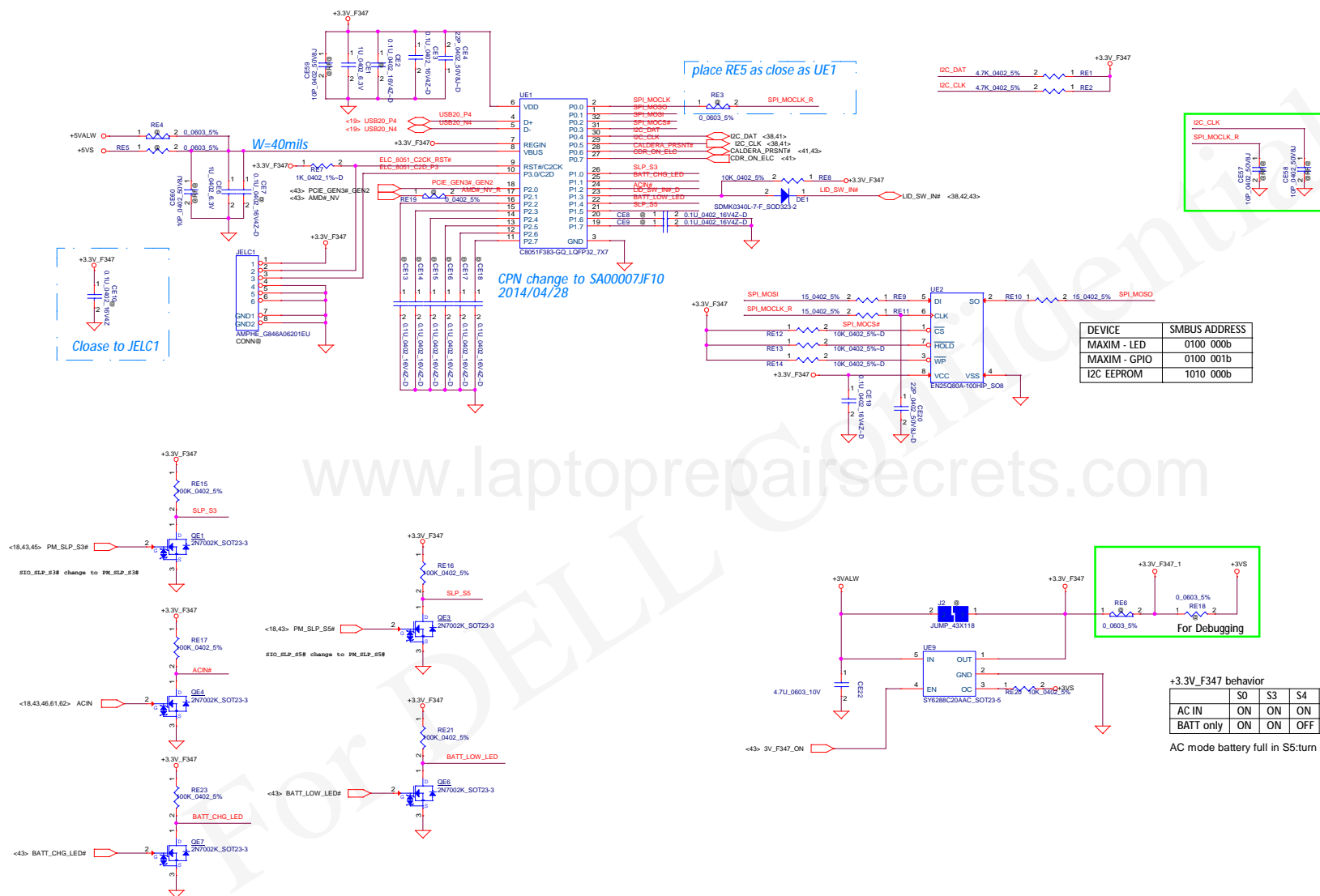
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Date: Wednesday, July 22, 2015				Sheet 35 of 78



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Size	Document Number	Rev	0.1	
LA-C912P		Date	Wednesday, July 22, 2015	Sheet 36 of 78



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				Rev 0.1
				Date: Wednesday, July 22, 2015 10:58:37 AM 37 of 78

MAX7313 change to TI TLC59116F PWM expander

Power LED

W=20mils

Logic up LED board

For IND/TP/HDD/PWR

To Hot Key

Power ON Circuit

ON/OFF switch

ON/OFF switch power button
Bottom Side pop only before MP

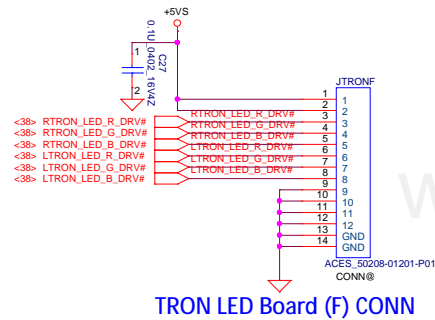
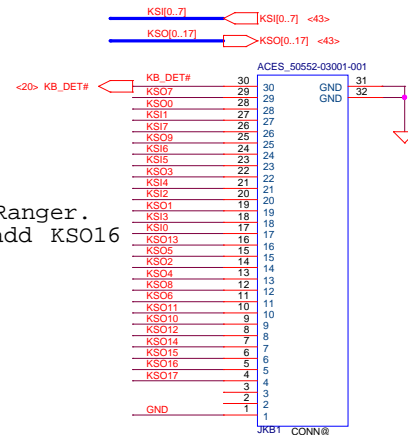
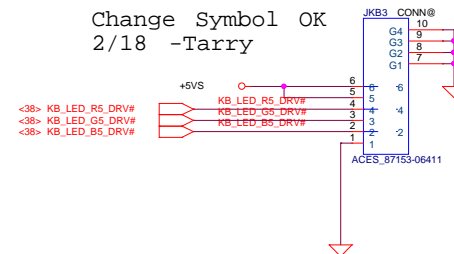
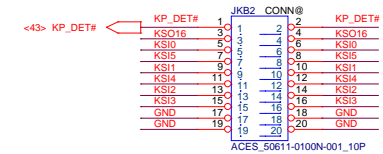
For TouchPAD

Touchpad LED circuit

Change Symbol OK
2/18 -Tarry

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				Sheet	LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	38 of 76

INT_KBD Conn.

Hot Key Conn.
PWMChange Symbol OK
2/18 -TarryHot Key Conn.
Key Pad

Compal Electronics, Inc.			
Title	KB/HotKey conn		
Size	Document	Number	Rev
		LA-C912P	0.1
Date:	Wednesday, July 22, 2015	Sheet	39 of 78

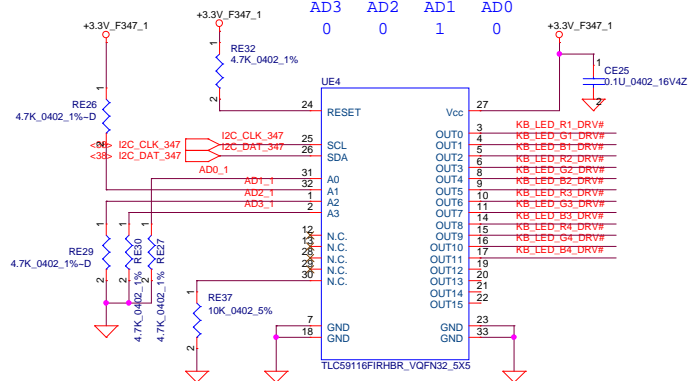
1/28 ADD

+5VS RE104 1 2 0.0603.5% 5V_LED
 +3VS RE105 1 2 0.0603.5% 5V_LED

K/B Backlight

AD3 AD2 AD1 AD0

0 0 1 0



KB BL LED

KB_LED_R1_DRV# A#

KB_LED_G1_DRV# A#

KB_LED_B1_DRV# A#

KB_LED_R2_DRV# A#

KB_LED_G2_DRV# A#

KB_LED_B2_DRV# A#

KB_LED_R3_DRV# A#

KB_LED_G3_DRV# A#

KB_LED_B3_DRV# A#

KB_LED_R4_DRV# A#

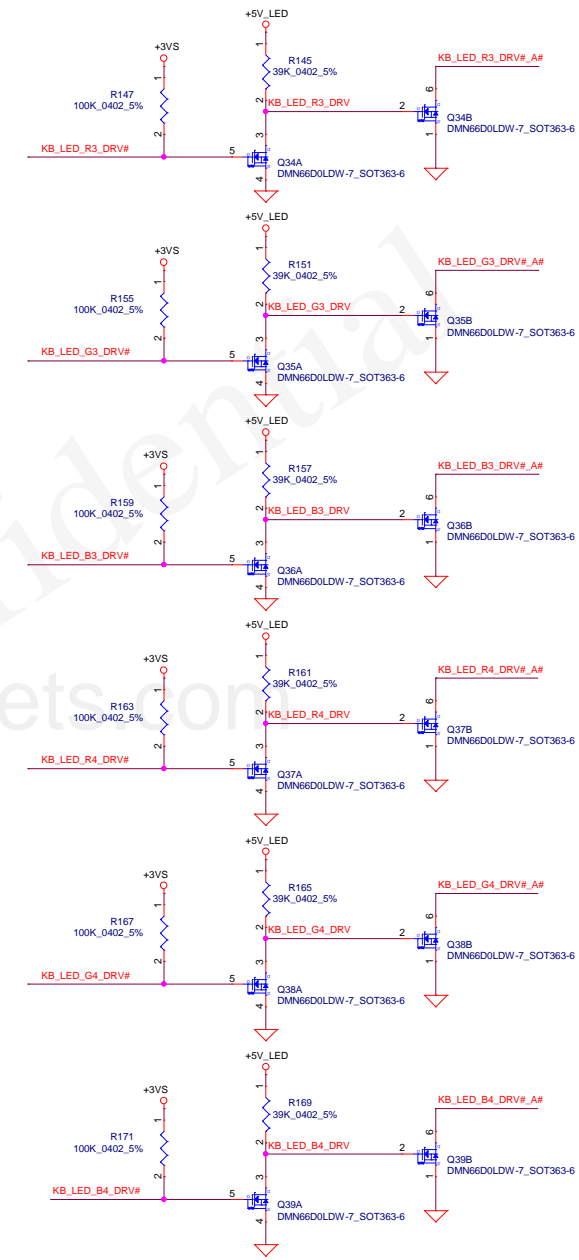
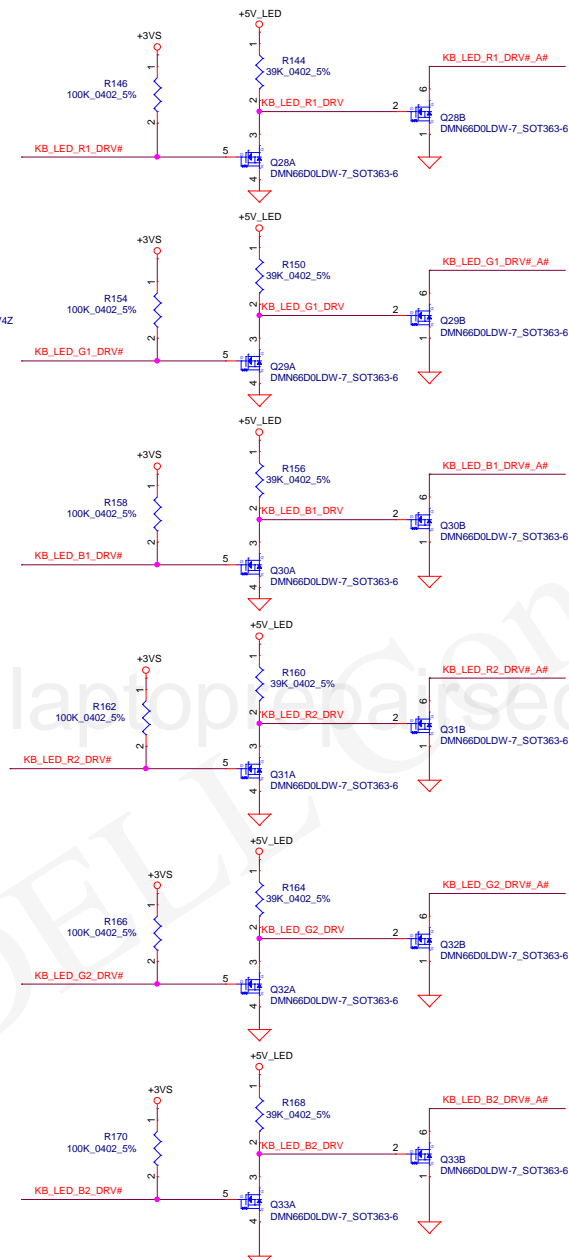
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KB_LED_B4_DRV# A#

KB_LED_R5_DRV# A#

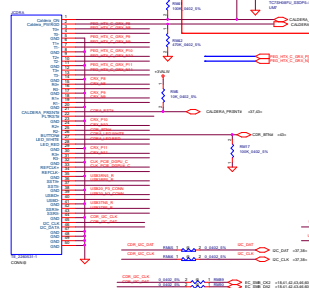
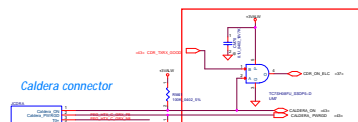
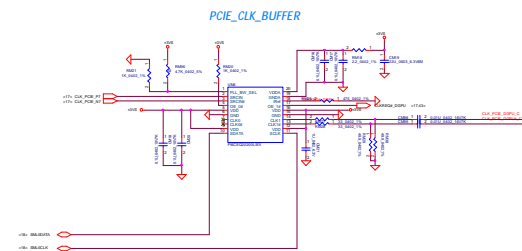
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KB_LED_B5_DRV# A#

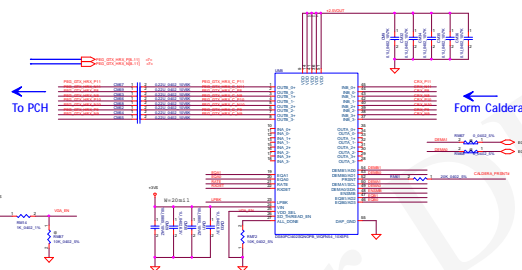
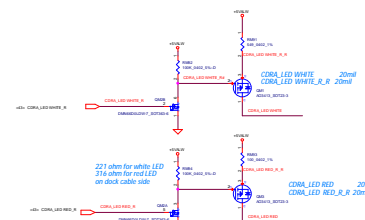
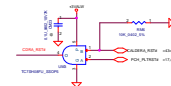


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Title			ELC(3)
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Date:	Wednesday, July 22, 2015	Sheet	40 of 78



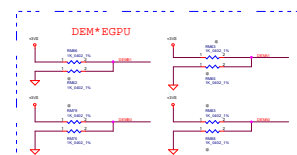
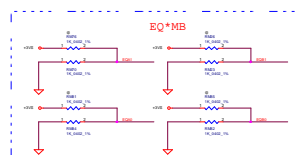
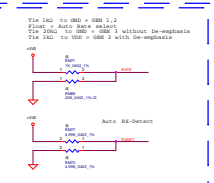
Follow ZAP00 design.



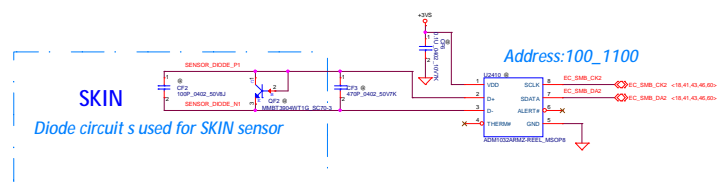
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2	0	0	-1.0	5 inch 5-6 trace
3	0	0	-1.0	5 inch 5-6 trace
4	1	8.0	-1.2	10 inch 5-6 trace
5	1	12.0	-1.2	20 inch 5-6 trace
6	1	16.0	-1.5	25 inch 5-6 trace
7	1	18.0	-1.7	30 inch 4-6 trace
8	1	18.0	-1.6	25 to 30 inch 4-6 trace
9	0	12.0	-1.8	30 inch 4-6 trace
10	0	12.0	-1.8	30 inch 4-6 trace
11	0	12.0	-1.4	30 inch 4-6 trace
12	0	12.0	-1.4	30 inch 4-6 trace
13	1	24.0	25.0	10m, 10m cable
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15	1	24.0	25.0	
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98	1	24.0	25.0	
99	1	24.0	25.0	
100	1	24.0	25.0	

level	DEMA SEAM	DEMA	DEMA dB	Suggested Use
1	0	0	0	<5 inch 4- or 6R trac
2	0	R	0	<5 inch 4- or 6R trac
3	0	F	-2.5	10 inch 4- or 6R trac
4	0	L	0	10 inch 4- or 6R trac
5	R	R	-1.5	10 inch 4- or 6R trac
6	R	F	-0.5	10 inch 4- or 6R trac
7	R	L	-2.5	10 inch 4- or 6R trac
8	F	0	-0.5	10 inch 4- or 6R trac
9	F	R	-1.5	10 inch 4- or 6R trac
10	F	L	-1.5	10 inch 4- or 6R trac
11	F	F	-1.5	10 inch 4- or 6R trac
12	F	L	-0	10 inch 4- or 6R trac
13	L	0	0	<5 inch 4- or 6R trac
14	L	R	-2.5	10 inch 4- or 6R trac
15	L	F	-0.5	10 inch 4- or 6R trac
16	L	L	-0.5	10 inch 4- or 6R trac

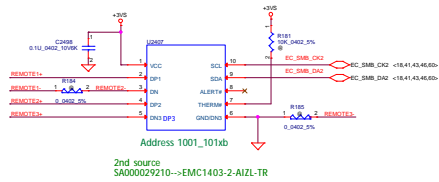
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2	1	100u to 0.01	10 inch 4- 10 tra
3	2	Float	10 inch 4- 10 tra
4	3	100u to 0.000	10 inch 4- 10 tra



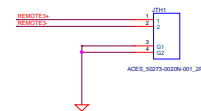
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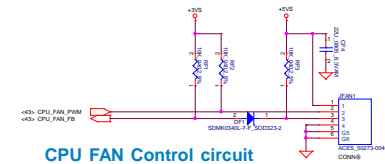
Fintek thermal sensor-> CPU core, DIMM



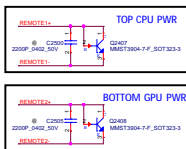
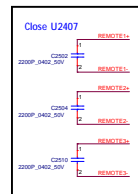
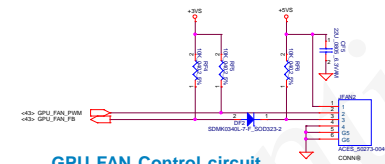
Thermal Board for SSD



CPU FAN Control circuit

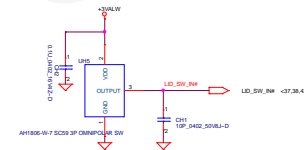


GPU FAN Control circuit



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:-8"

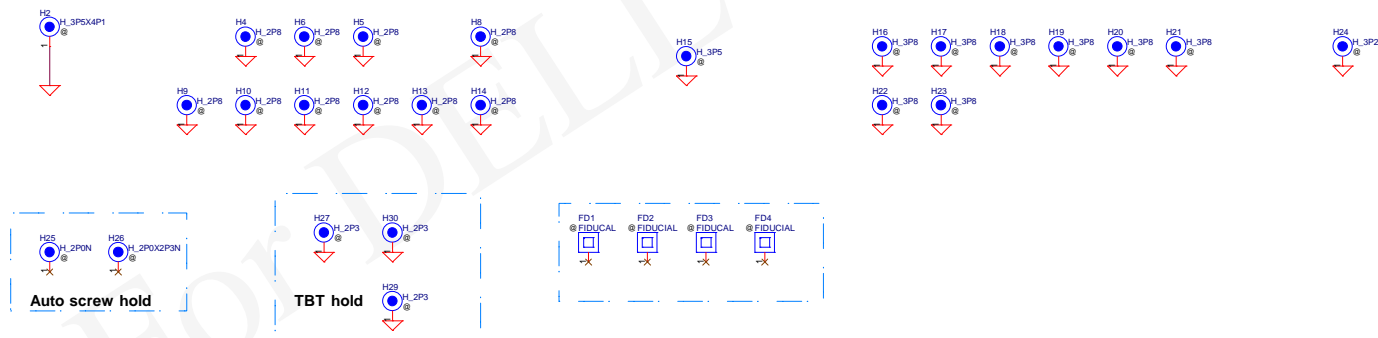
Lid Switch (Hall Effect Switch)



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		1A-C912P
		DATE: 2016/01/30

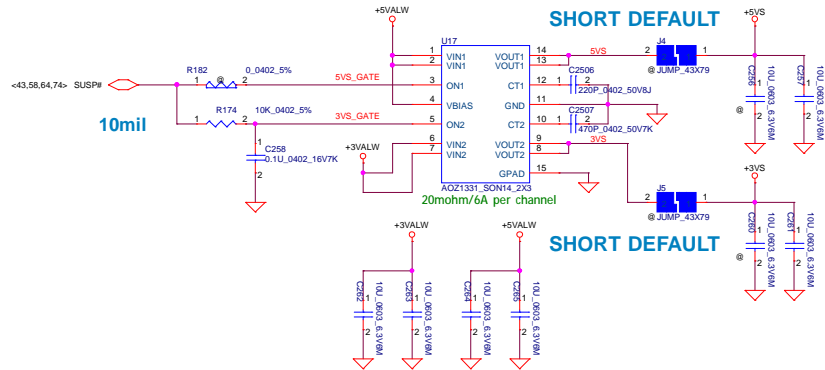


Screw Hole

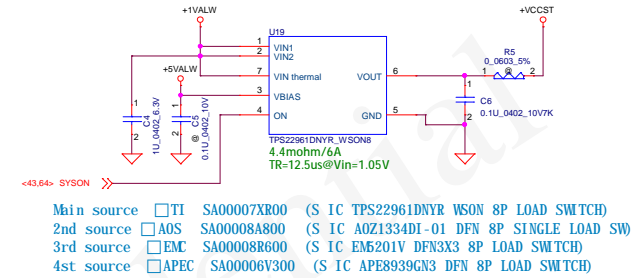


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				Document Number
				LA-C912P
				Rev
				0.1
				Date: Wednesday, July 22, 2015
				Sheet 44 of 78

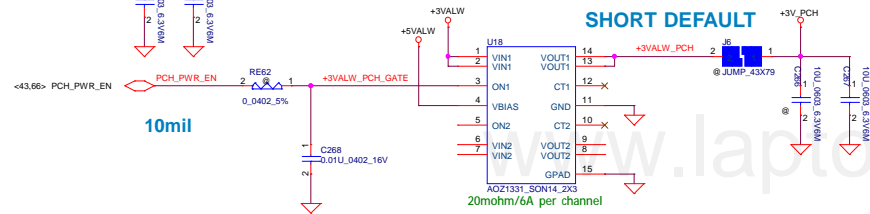
+5VS and +3VS switch



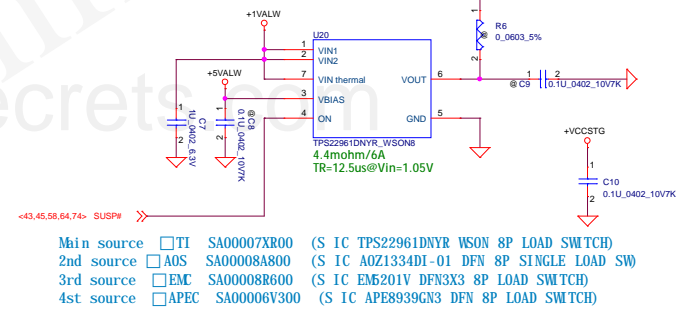
+VCCST Load Switch



+3VALW_PCH switch



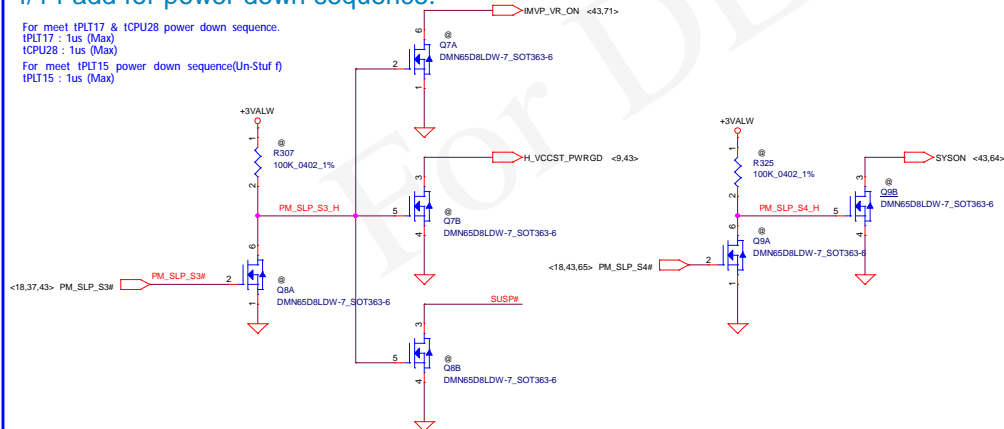
+VCCSTG source



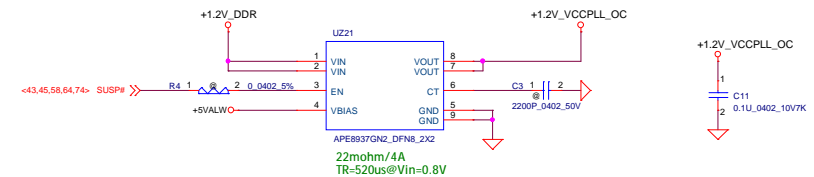
4/14 add for power down sequence.

For meet tPLT17 & tCPU28 power down sequence.
 tPLT17 : 1us (Max)
 tCPU28 : 1us (Max)

For meet tPLT15 power down sequence(Un-Stuf f)
 tPLT15 : 1us (Max)

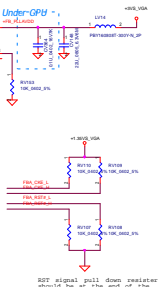


+1.2V_VCCPLL_OC



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				DC/DC Interface	
				Size	Document Number
				LA-C912P	
				Date	Wednesday, July 22, 2015
				Sheet	45 of 78
				Rev	0.1



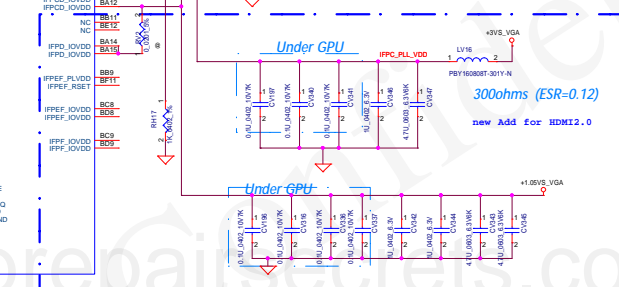
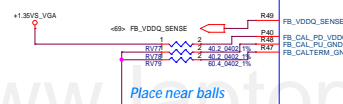


Node # ASB4-104	0...31	Node # ASB4-104	32...63
OS025	OS*	OS*	OS*
OS026	A1_A3	OS027	A1_A3
OS028	A2_A3	OS029	A2_A3
OS030	A4_A3	OS031	A4_A3
OS032	A5_A3	OS033	A5_A3
OS04	HE*	OS021	HE*
OS08	A7_A8	OS022	A7_A8
OS09	A1_A3	OS023	A1_A3
OS10	AB*	OS024	AB*
OS09	A12_A10	OS025	A12_A10
OS10	A10_A10	OS026	A10_A10
OS011	A1_A3	OS027	A1_A3
OS012	AB*	OS028	AB*
OS013	EB*	OS029	EB*
OS014	CE*	OS030	CE*
OS015	CAD*	OS031	CAD*
OS017	OS		
OS019	OS		
OS020	OS		
OS035	OS020		
OS035	OS020		

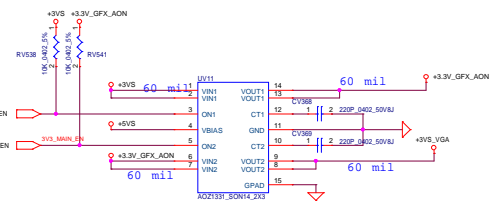
Node #	Mode	Q ₁ , J1	Node #	Mode	Q ₂ , J2
CHD0	CAS*	CHD16	CAS*		
CHD1	CE1*	CHD17	CE1*		
CHD2	R2P*	CHD18	R2P*		
CHD3	RA*	CHD19	RA*		
CHD4	A1_A9	CHD20	A1_A9		
CHD5	AS_A10	CHD21	AS_A10		
CHD6	A12_A10	CHD22	A12_A10		
CHD7	CE*	CHD23	CE*		
CHD8	A1_A11	CHD24	A1_A11		
CHD9	AS_A11	CHD25	AS_A11		
CHD10	WE*	CHD26	WE*		
CHD11	A1_A81	CHD27	A5_A81		
CHD12	A1_A82	CHD28	A5_A82		
CHD13	A1_A83	CHD29	A5_A83		
CHD14	A1_A84	CHD30	A5_A84		
CHD15	CE*	CHD31	CE*		
CHD16	WE*	WE*			
CHD17	WE*	WE*			
CHD18	WE*	WE*			
CHD19	WE*	WE*			
CHD20	WE*	WE*			
CHD21	WE*	WE*			
CHD22	WE*	WE*			
CHD23	WE*	WE*			
CHD24	WE*	WE*			
CHD25	WE*	WE*			
CHD26	WE*	WE*			
CHD27	WE*	WE*			
CHD28	WE*	WE*			
CHD29	WE*	WE*			
CHD30	WE*	WE*			
CHD31	WE*	WE*			

Title	<i>N15P-GX (5/5) POWER/ GND</i>	
Issue	Component	Material
Design	<i>LA-C912P</i>	

1.05V	22uF	10uF	4.7uF	1uF	0.1uF
SP_PLIVDD VID_PLIVDD	1		1		1X2
GPU_PLIAVDD	1				5



+3VS VGA / +3.3V GFX AON

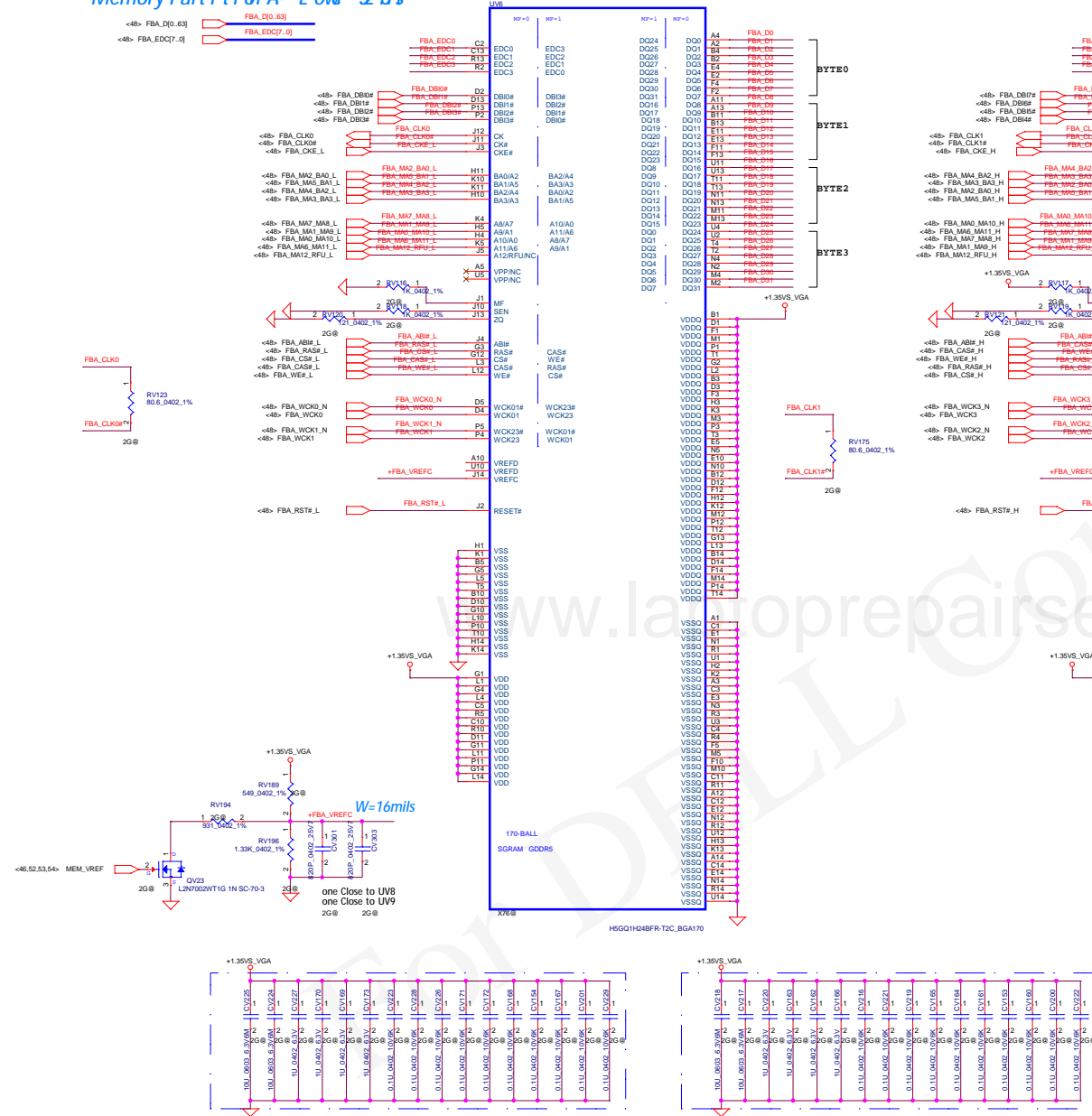


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				Docu	LA-C192P
				Date:	Wednesday, July 22, 2015
				Sheet	49 of 78

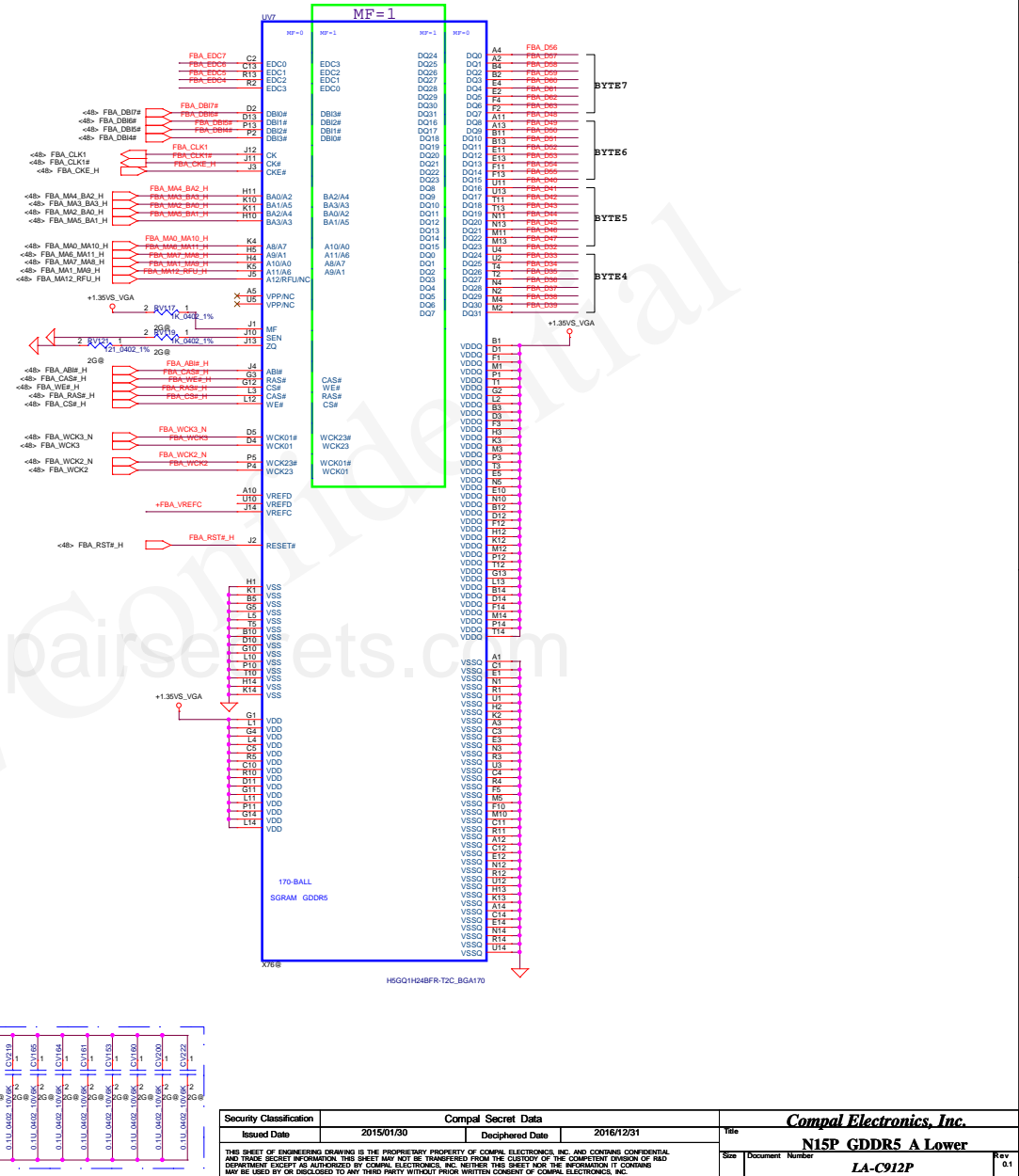


Memory Partition A- Lower 32bits

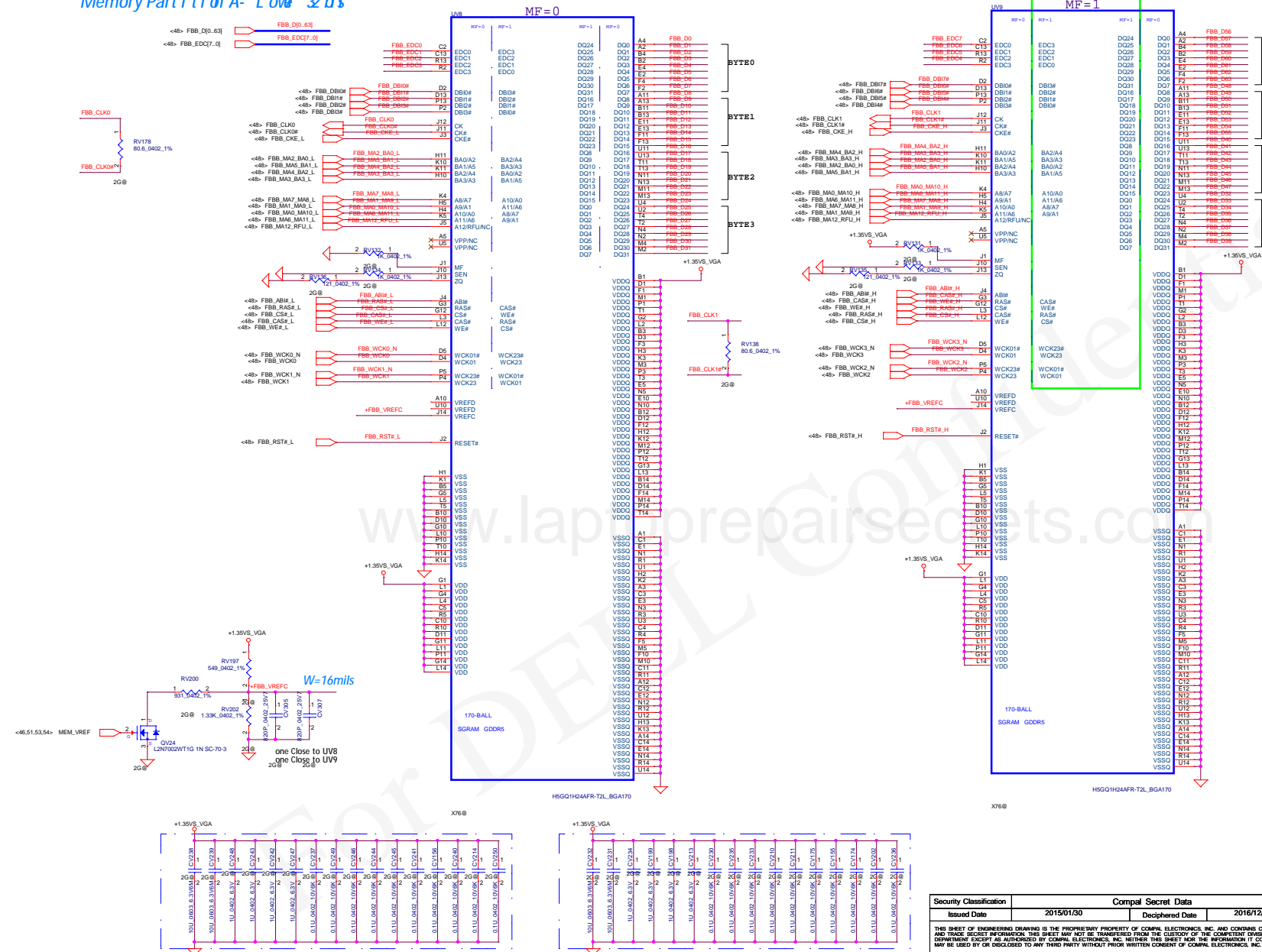
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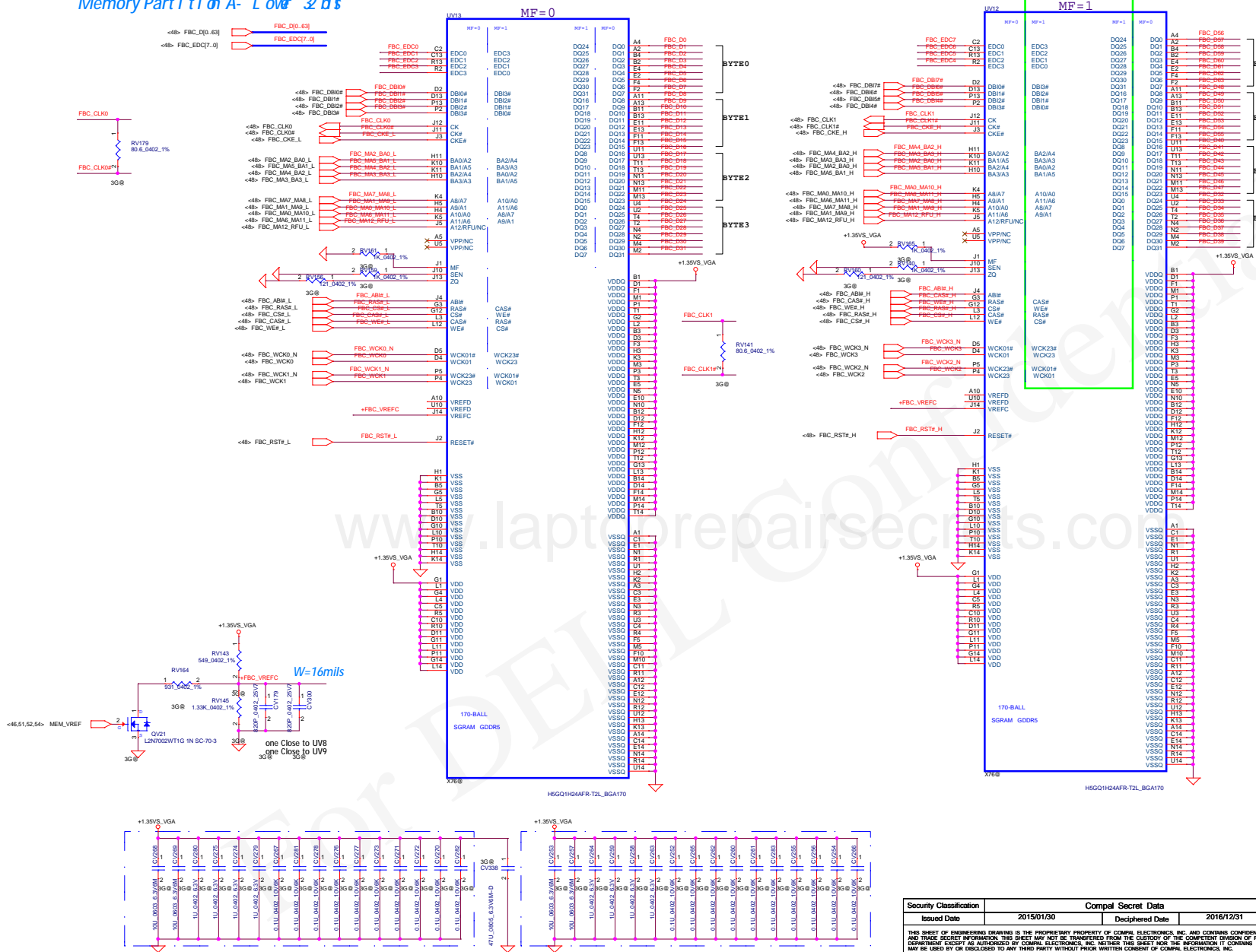
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Memory Partition A - Lower 2B's

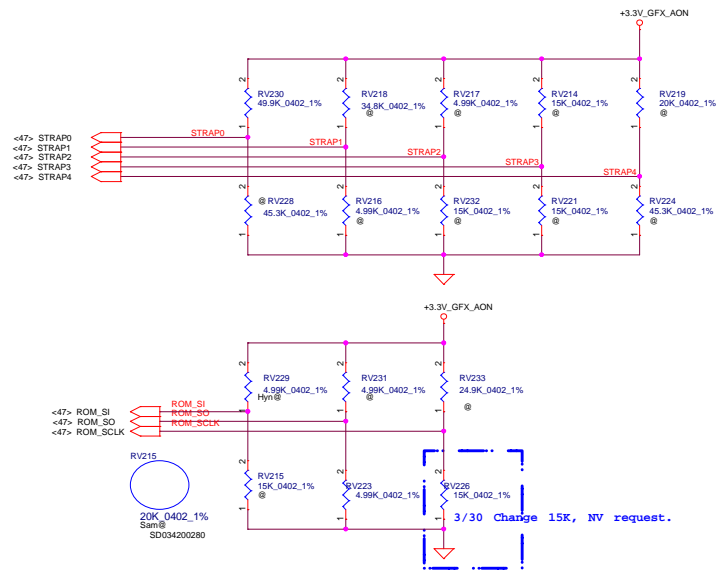


Memory Partition A- Lower 32 bits



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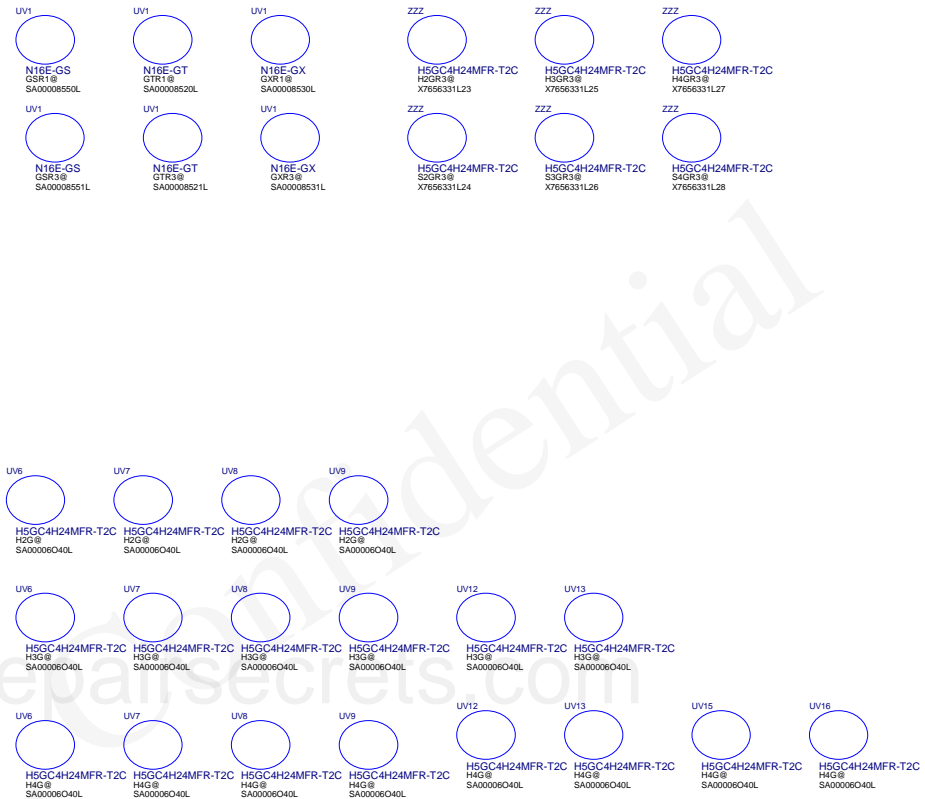


R_pu

VRAM	Strap	ROM-SI
Hynix H5GC4H24MFR-T2C	0x2	PL 15K
Samsung K4G41325FC-HC03	0x3	PL 20K
Hynix H5GC4H24AJR-R0C	0x8	PH 5K

Set as Hynix H5GC4H24AJR-T2C @5G

	P1 to 3V3	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



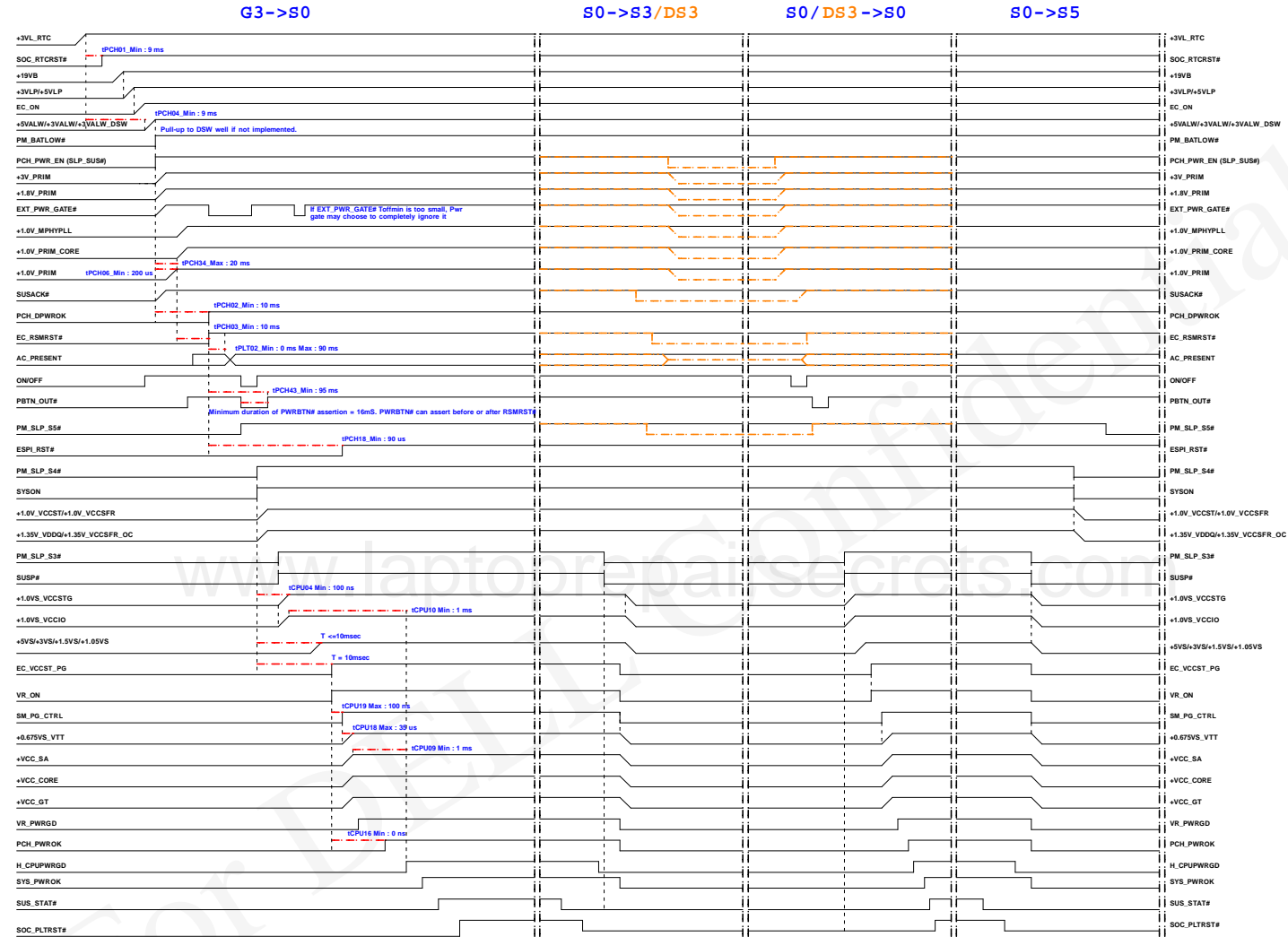
PCI_DEVICE

SUB_VENDER
0- w/o dGPU ROM
1-w/ dGPU ROMFB[1:0]
0-Reserved
1-Reserved
2-256M
3-ReservedVGA_DEVICE
0- Non-permy 3D
1-SMB_ALT_ADDR
0-0x9E
1-0x9C(Multi i- GPU)PEX_PLL_EN_TERM
0-Disable
1-Enable3GIO_PADCFG
0110-Gen1/Gen2
0000-Gen3PCI_MAX_SPEED
0-booting to P0E Gen1
1-booting to P0E Gen2/Gen3PCI_SPEED_CHNAGE_GEN3
0-Disable PCI Gen3
1-Enable PCI Gen3

Physical Strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDER	PCI_DEVICE[5]	PEX_PLL_EN_TERM
ROM_SO	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_CFG[3]	3GIO_CFG[2]	3GIO_CFG[1]	3GIO_CFG[0]
STRAP2	PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHNAGE_GEN3	PCI_MAX_SPEED	DP_PLL_VDD33V

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NISP-GX (I/5) PEG & DAC				Sheet 55 of 78
Date: Wednesday, July 22, 2016				

[AAX06-PWR Sequence_SKL-H 4+4_DDR4_Volume_NON CS]



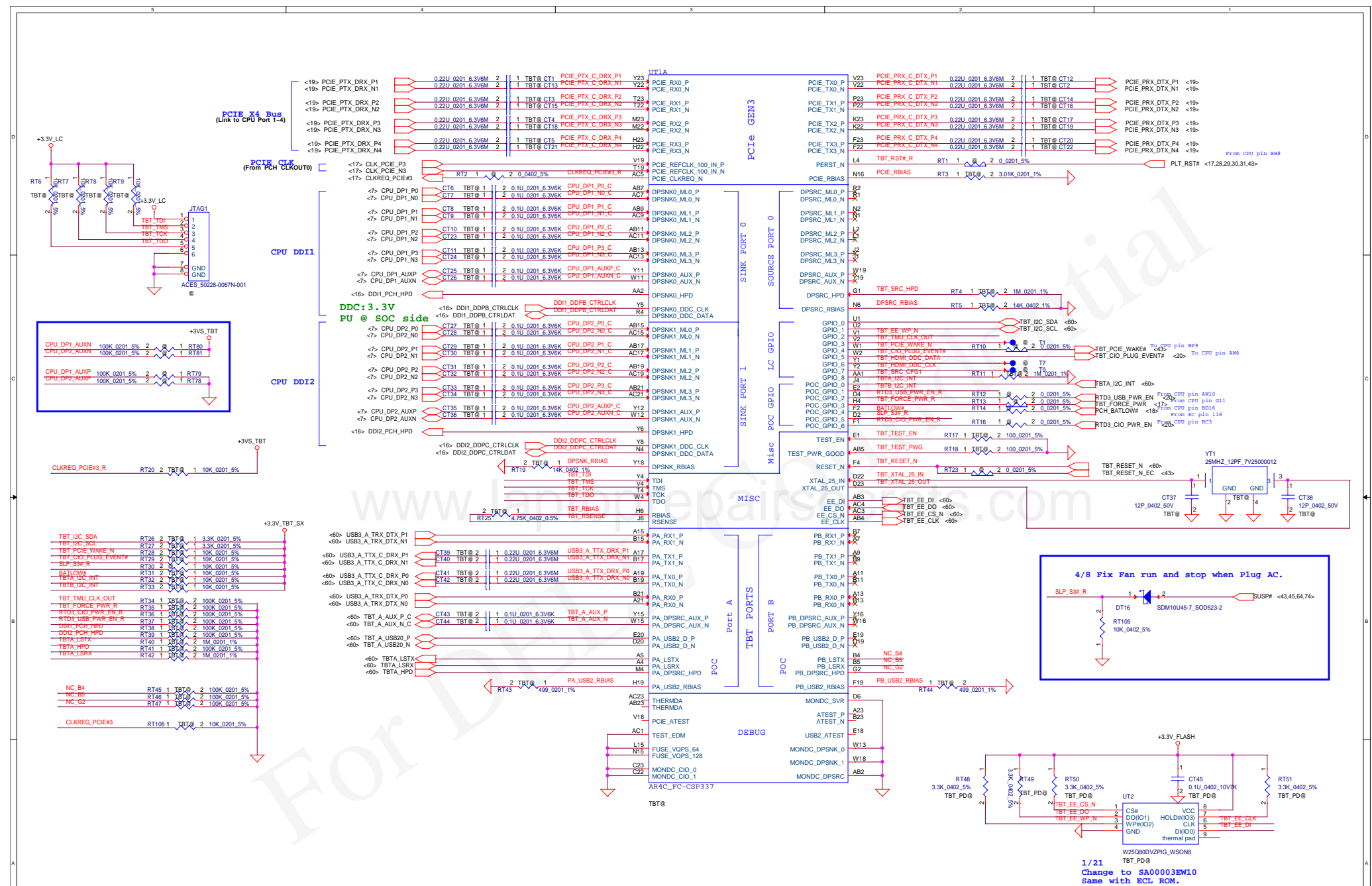
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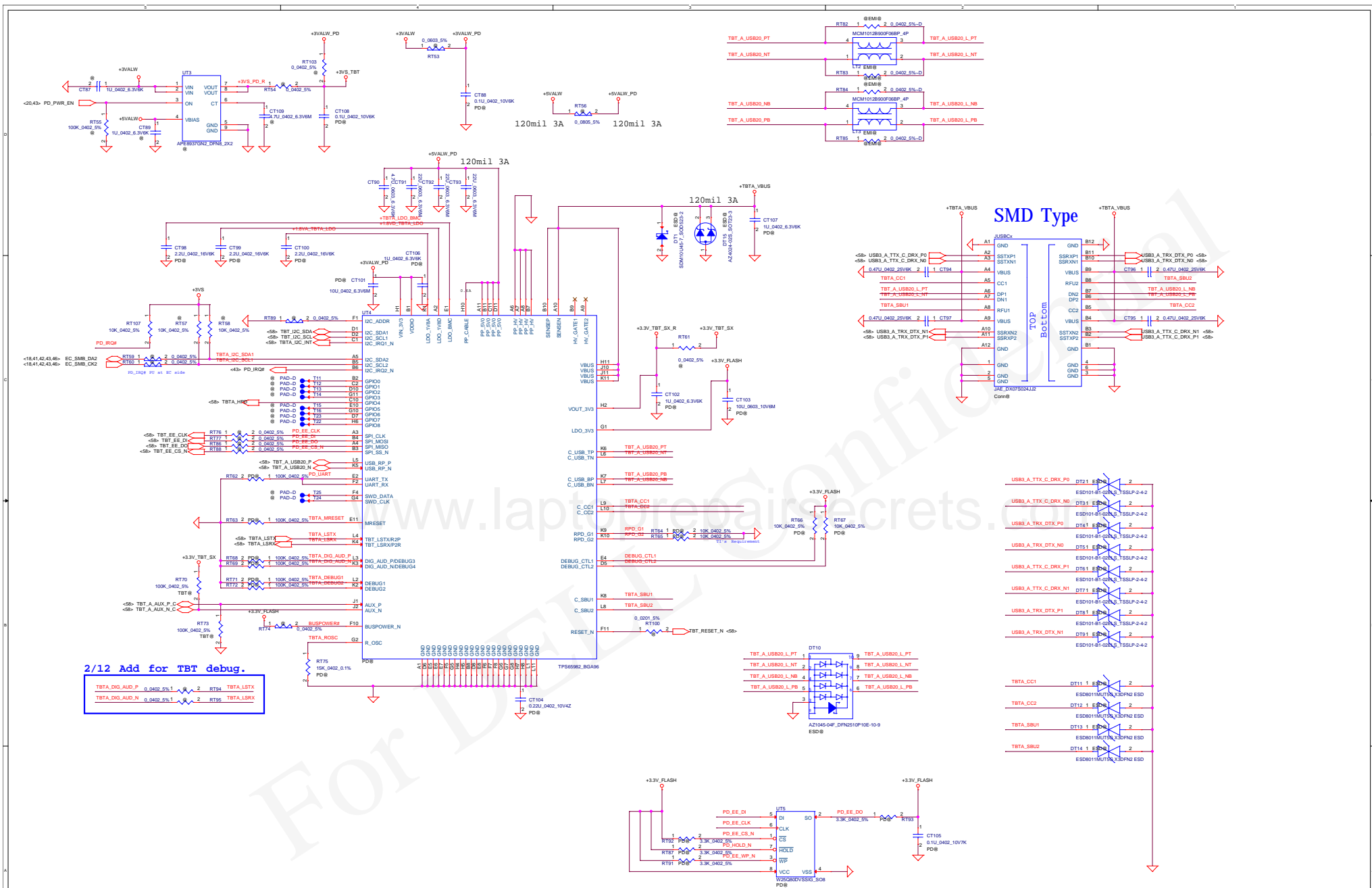
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				Document Number	
				LA-C912P	
Date: Wednesday, July 22, 2015				Sheet 67 of 78	Rev 0.1

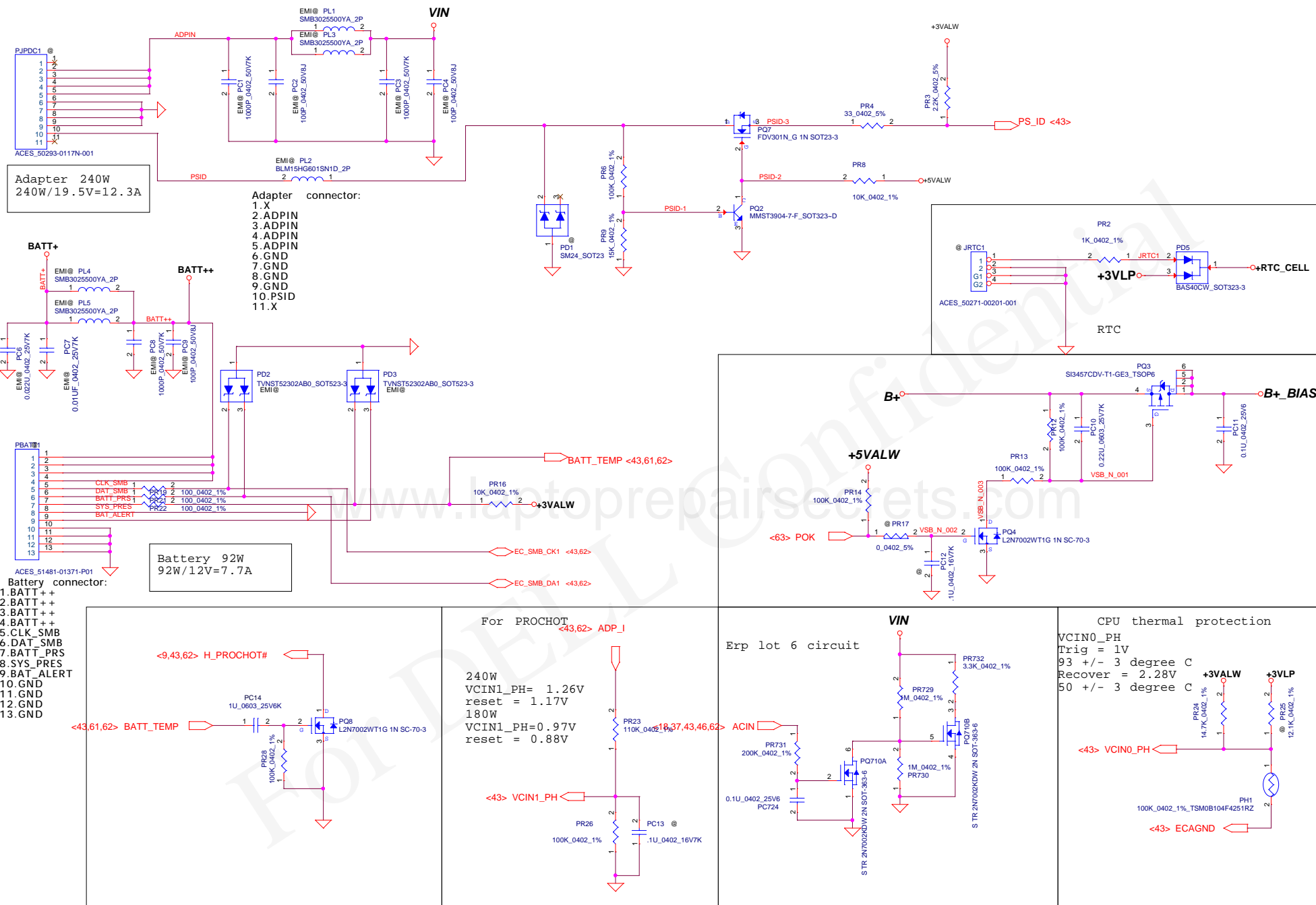


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				Date	Wednesday, July 22, 2015
				Sheet	58 of 78

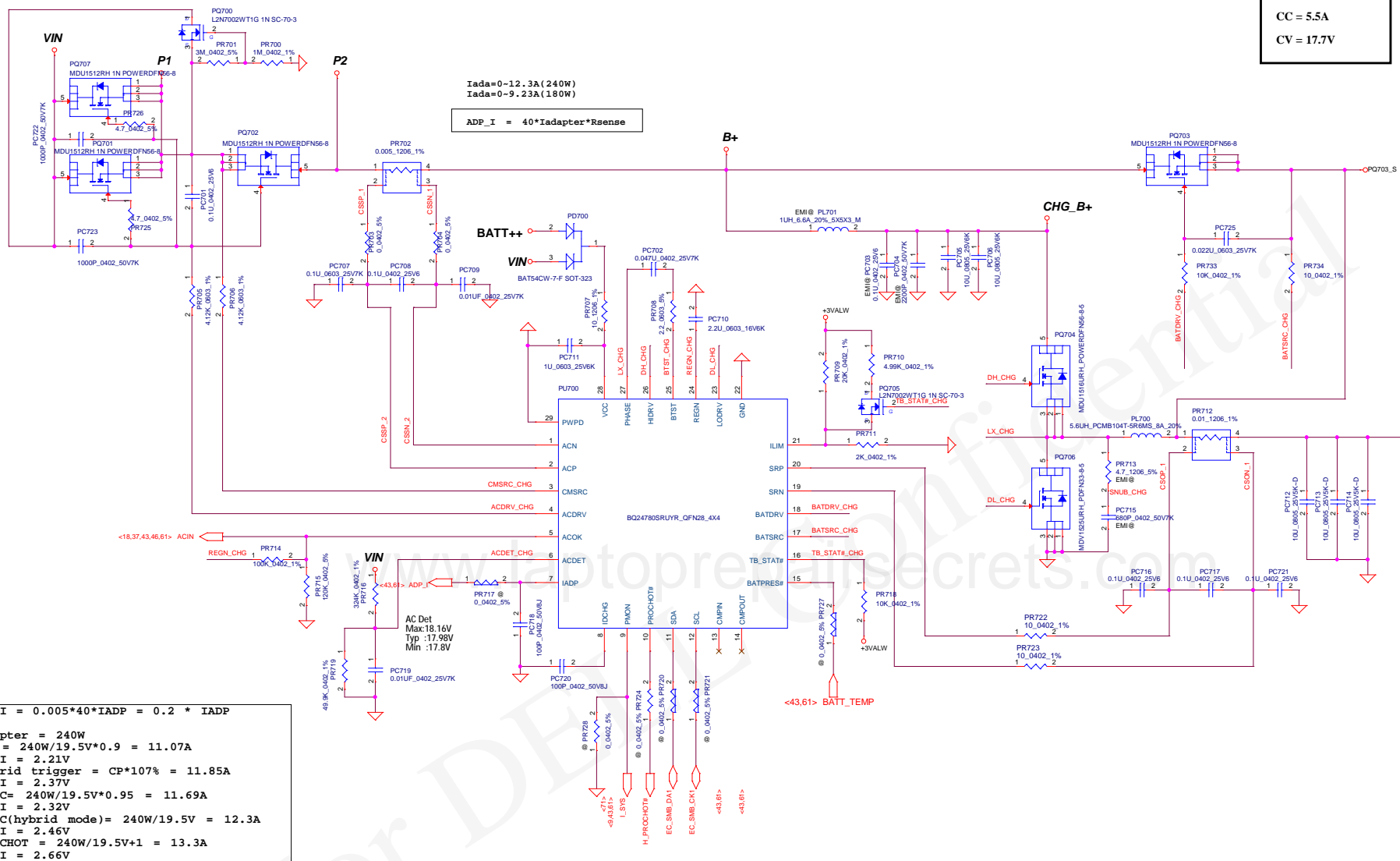




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Date Wednesday, July 23, 2015				Sheet 67	of 78

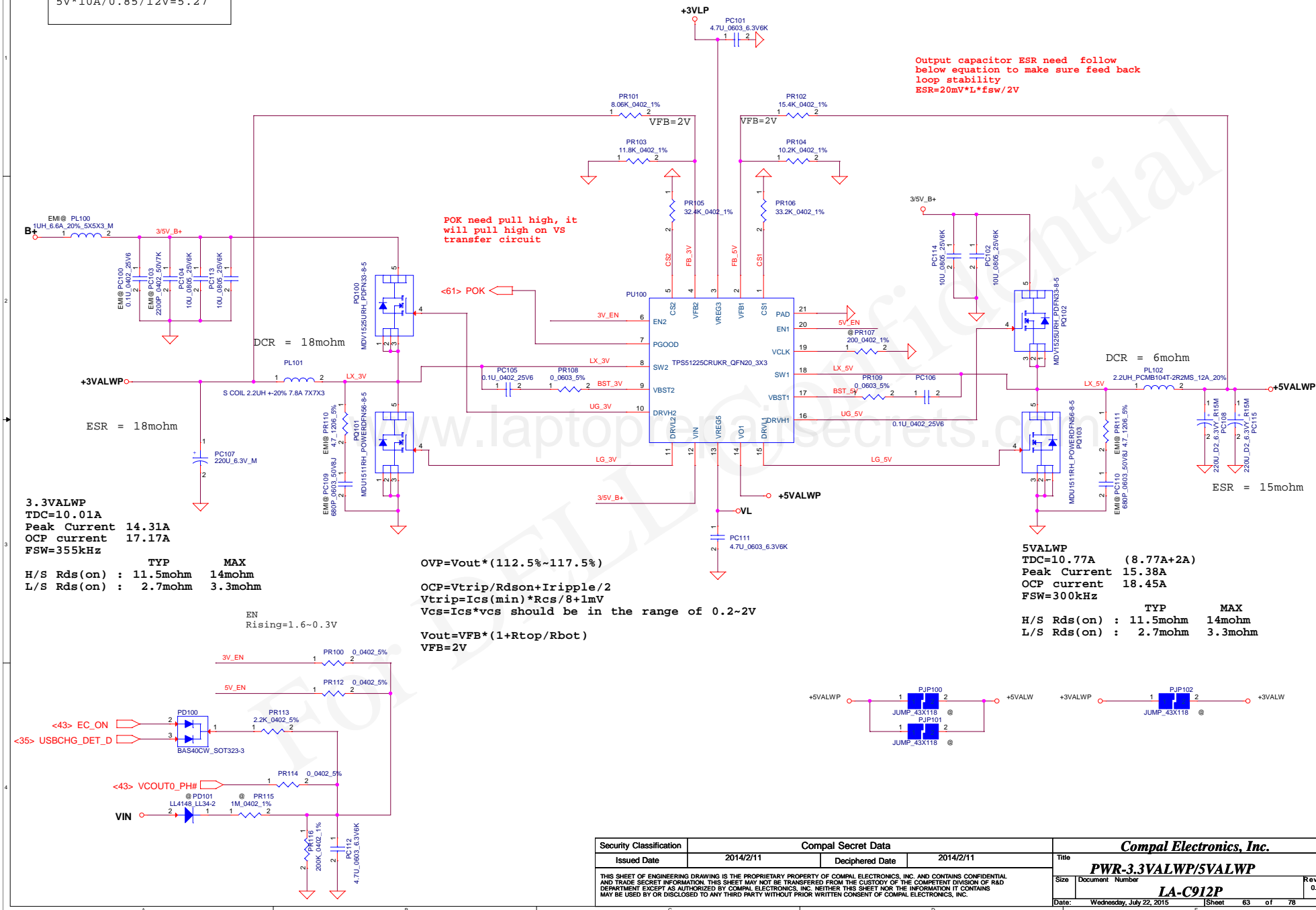


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Size	Document	Number	Rev	0.1
Date: Wednesday, July 22, 2015		Sheet 61 of 78		



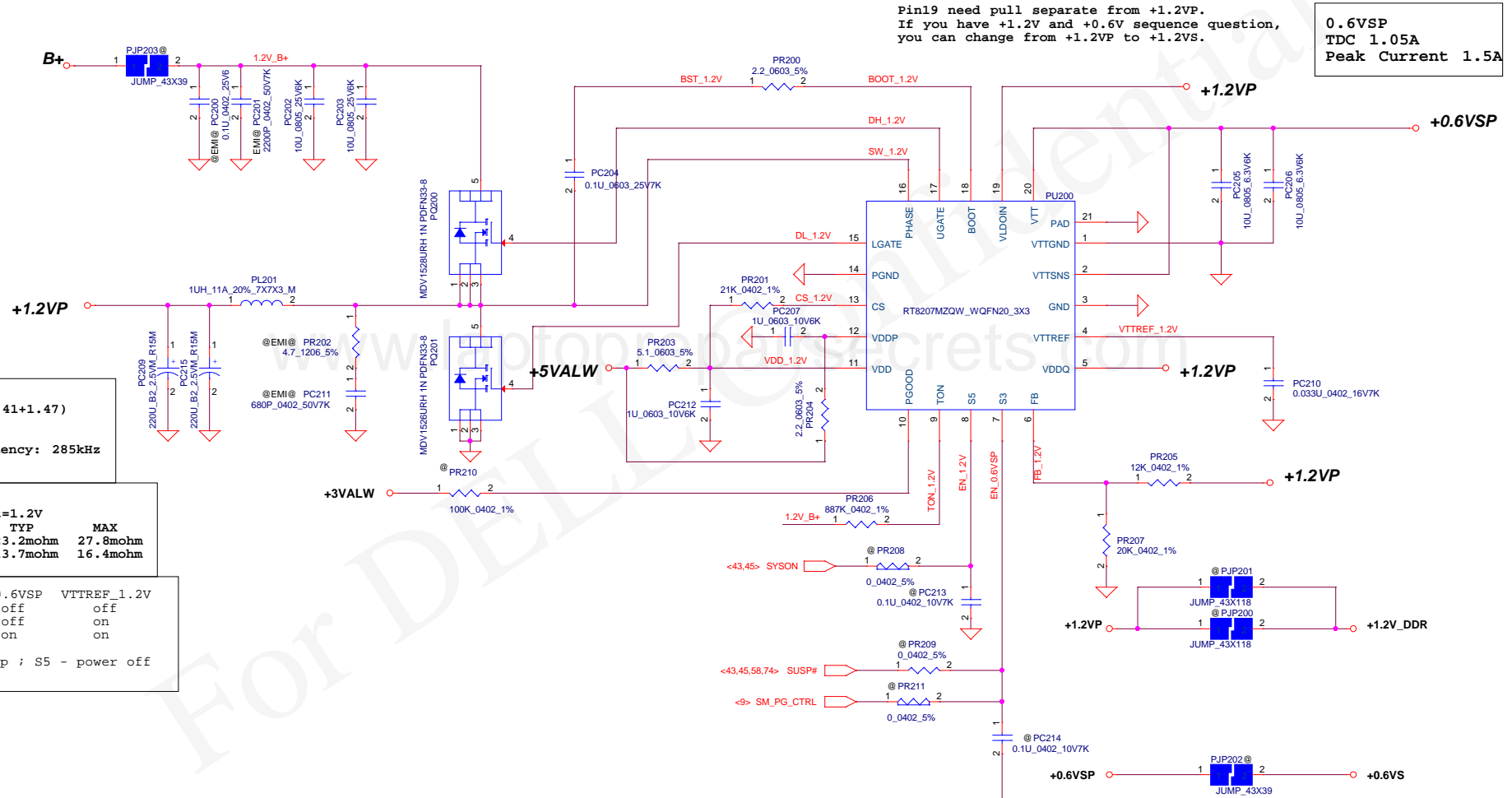
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LA-C912P				Rev 0.1
Date: Wednesday, July 22, 2015				Sheet 02 of 78

Input Current: 7.5A
 $3.3V \times 10A / 0.85 / 12V = 2.23$
 $5V \times 10A / 0.85 / 12V = 5.27$

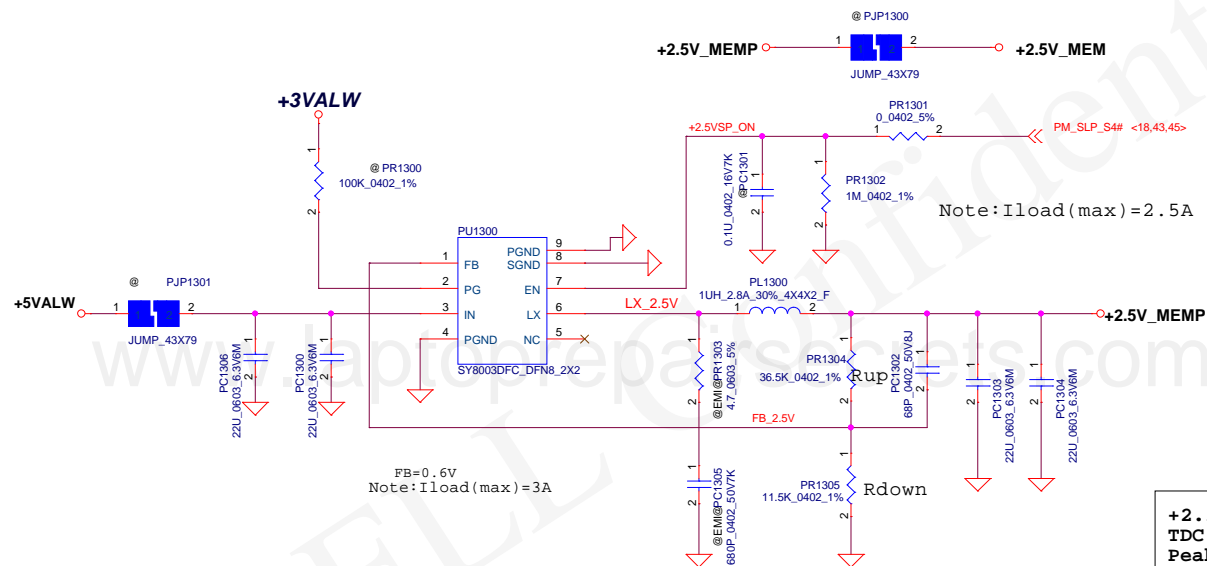


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2014/2/11		2014/2/11		PWR-3.3VALWP/5VALWP	
Size		Document Number		Rev	
1		LA-C912P		0.1	
Date		Wednesday, July 22, 2015		Sheet	
63		of		78	

Input Current: 1A
 $1.2V \times 8.88A / 0.85 / 12V = 1$



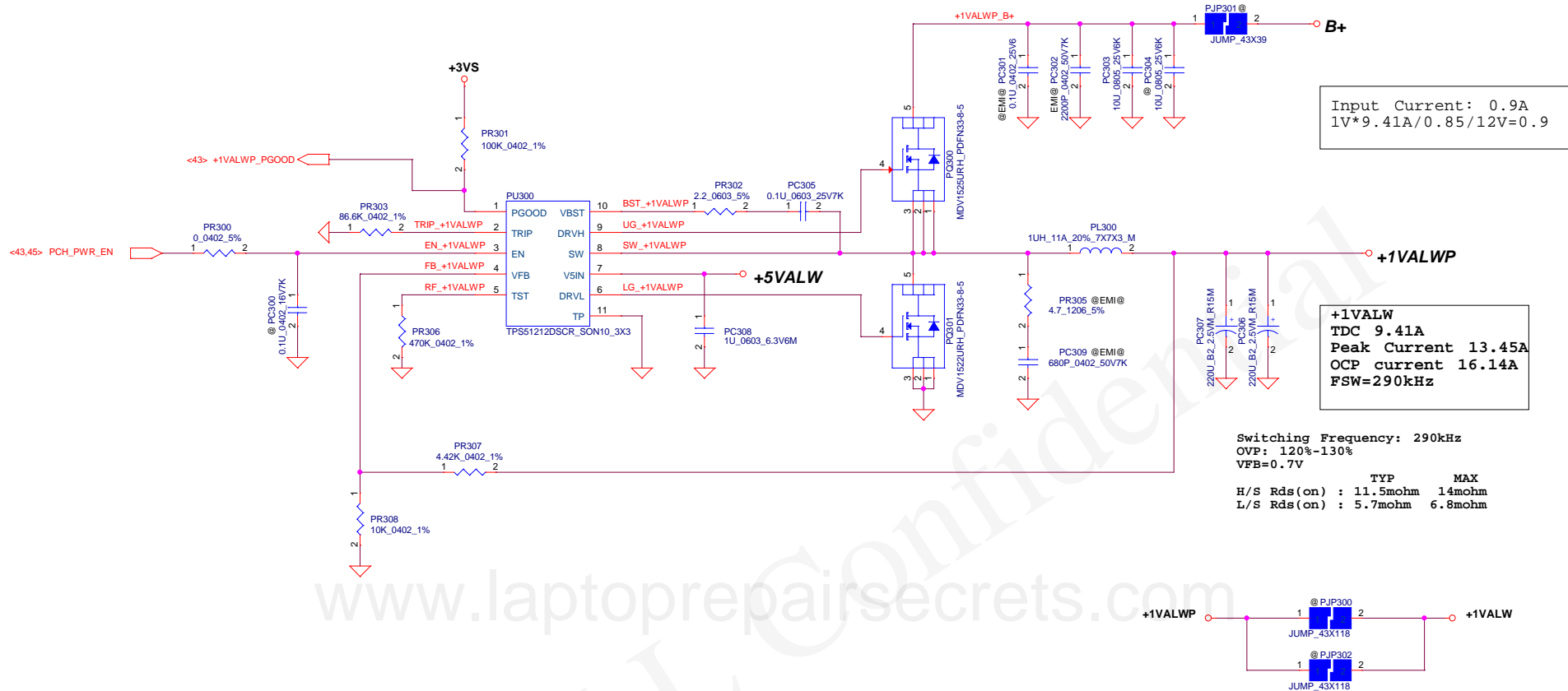
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Size	Document	Number	LA-C912P	Rev 0.1
Date:	Wednesday, July 22, 2015	Sheet	64	of 78



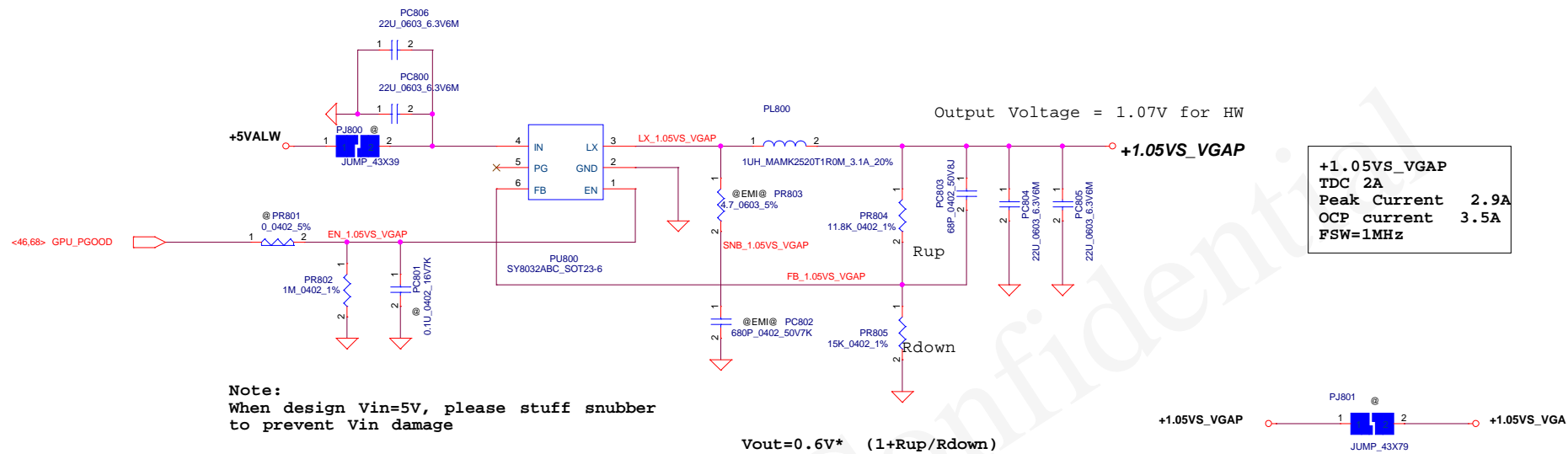
Note:
When design $V_{in}=5V$, please stuff snubber
to prevent V_{in} damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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				Document Number	0.1
				Date:	Wednesday, July 22, 2015
				Sheet	65 of 78
				LA-C912P	



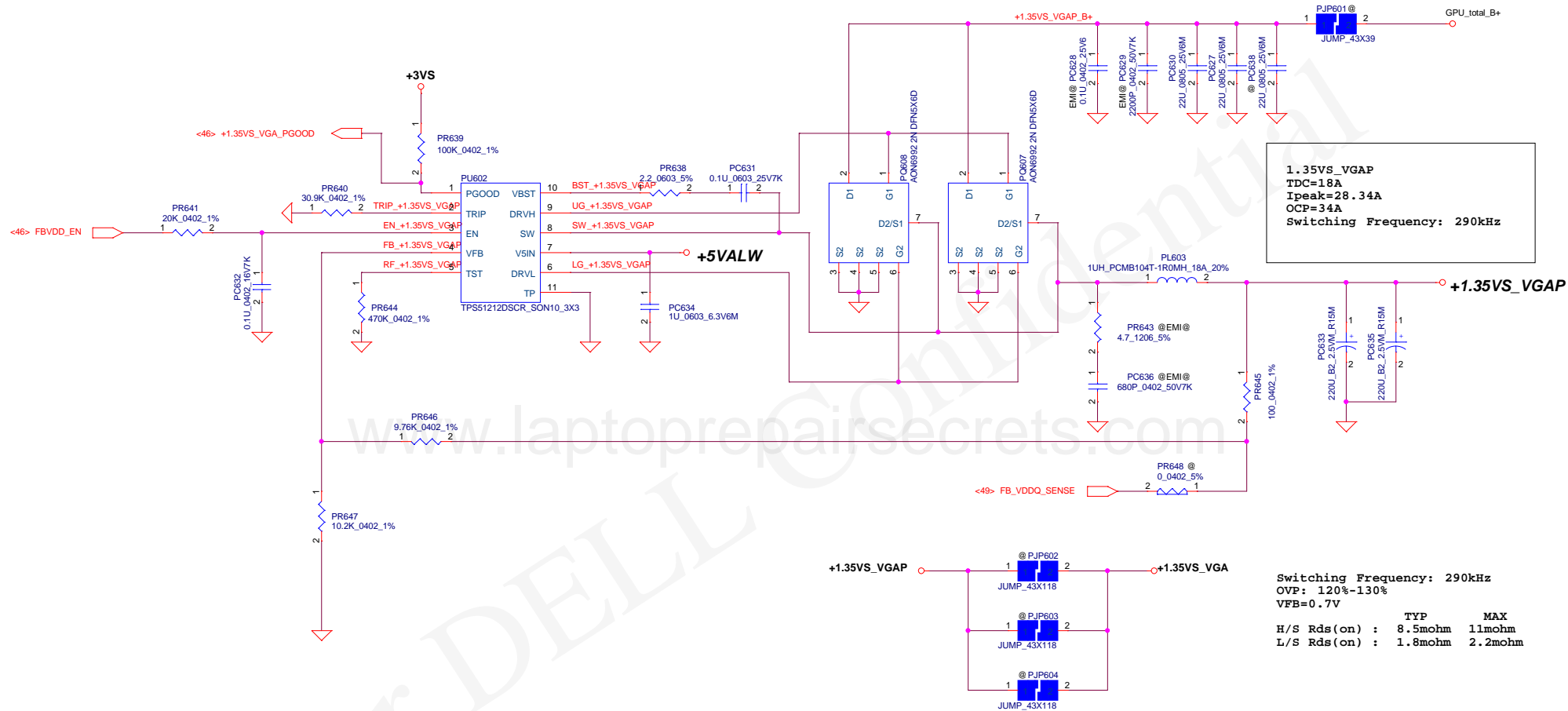
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				LA-C912P	
				Date	Wednesday, July 22, 2015
				Sheet	66 of 78
				Rev	0.1



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					LA-C912P	0.1
				Date:	Wednesday, July 22, 2015	Sheet 67 of 78





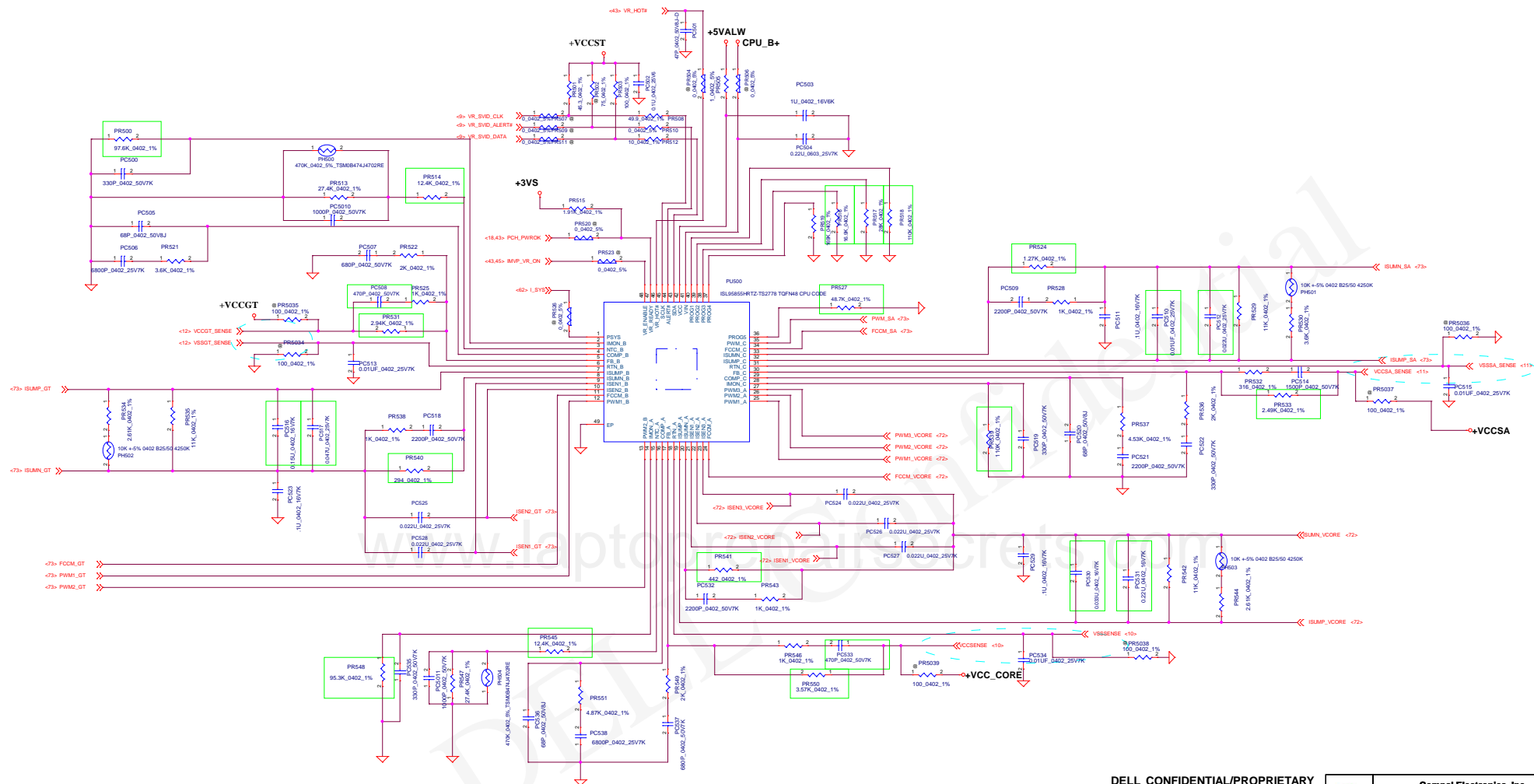
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						Size		Document Number		Rev	
								LA-C912P		0.1	
						Date:		Wednesday, July 22, 2015		Sheet 69 of 78	

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A vertical number line with points A, B, C, and D. Point A is at the bottom, followed by B, then C, and D at the top. There are tick marks for each point. A horizontal line segment is drawn between points B and C.

A vertical number line with points A, B, C, and D. Point A is at the bottom, followed by B, then C, and D at the top. There are tick marks for each point. A horizontal line segment is drawn between points B and C.



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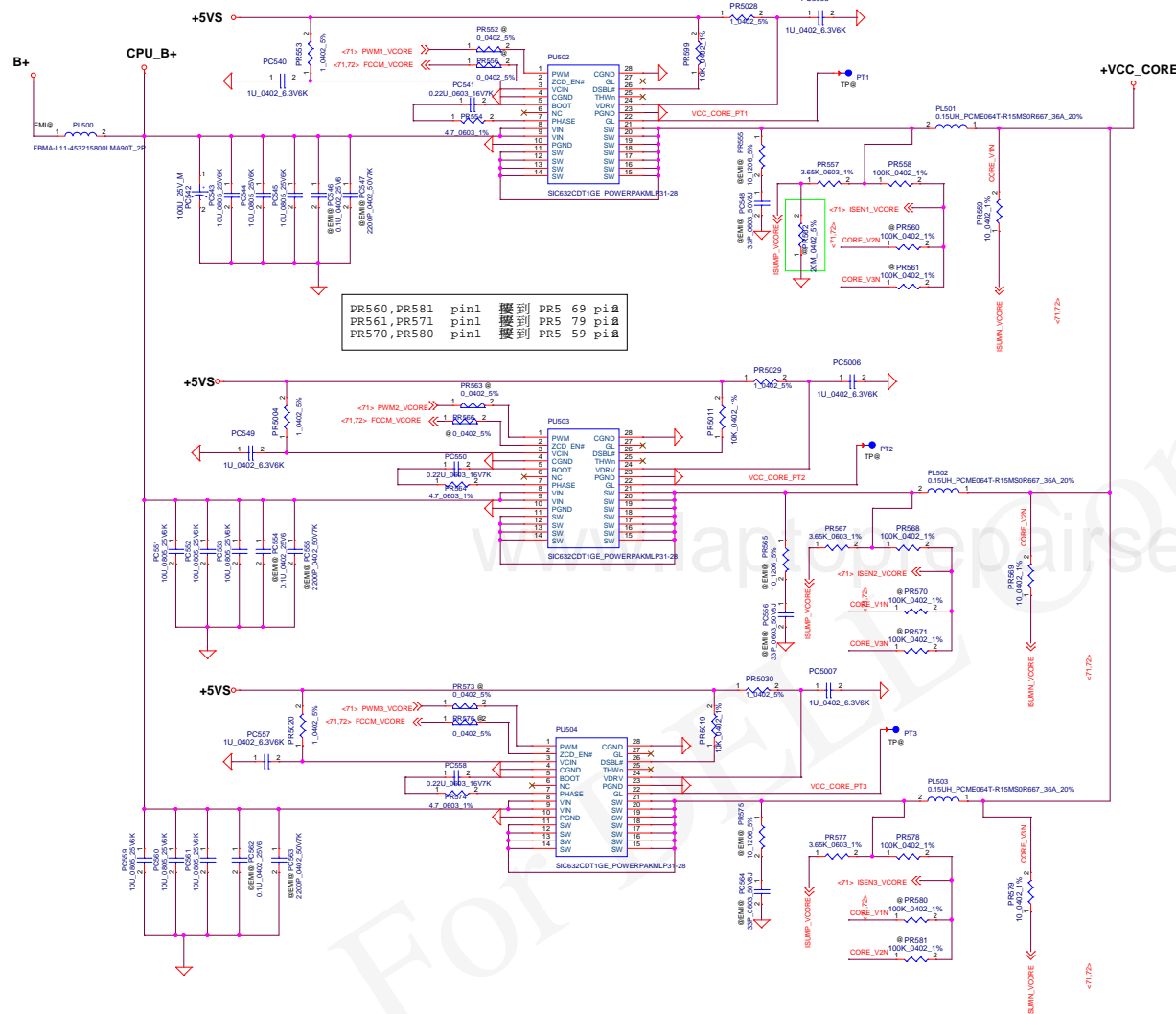
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Compaq Electronics, Inc.	
PWR_VCORE_ISL95855	
Rev	0.1
Doc Number	LA-C912P
Date	Wednesday, July 23, 2003
Page	7.1 of 7.8

Input Current: 8.2A
 $1.5V \times 56A / 0.85 / 12V = 8.2$

VCC_CORE
 TDC PL2 :56A
 Peak Current 68A
 OCP Current 81.6A
 DCR 0.66mohm +/-7%
 Load Line 1.8mV/A



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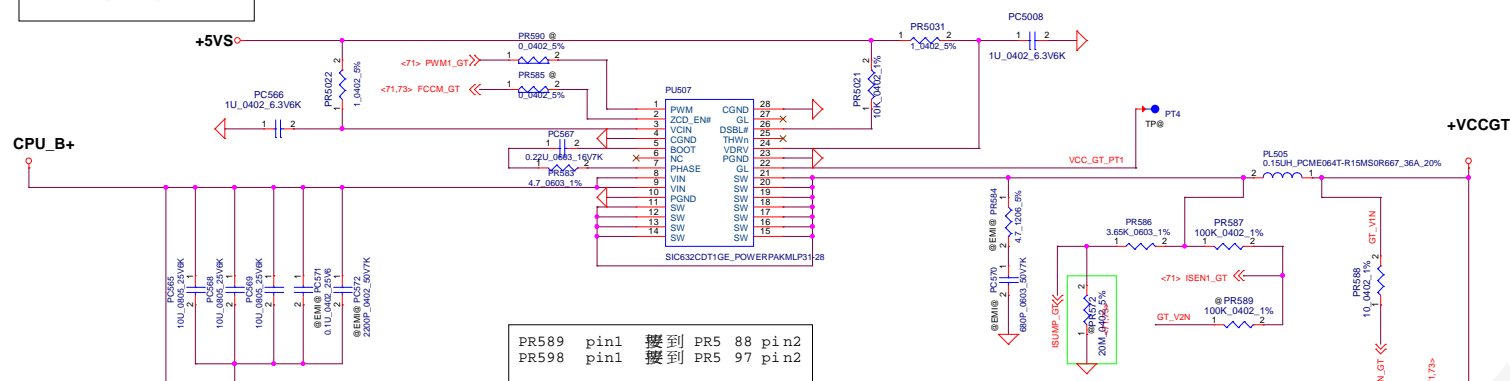


Compaq Electronics, Inc.

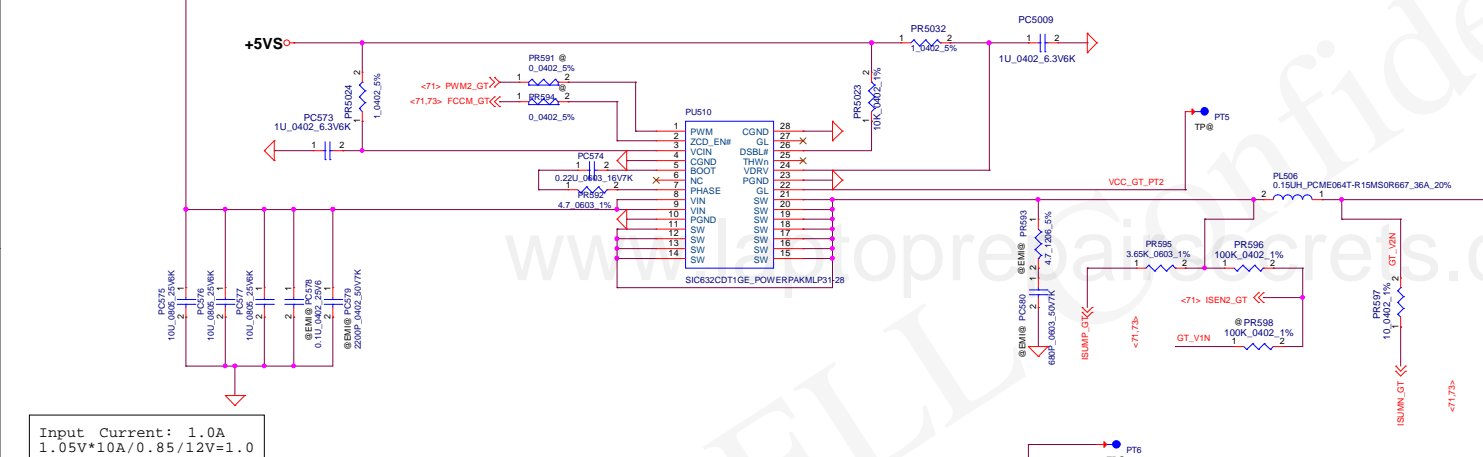
PWR_VCORE_VCORE

LA-C912P

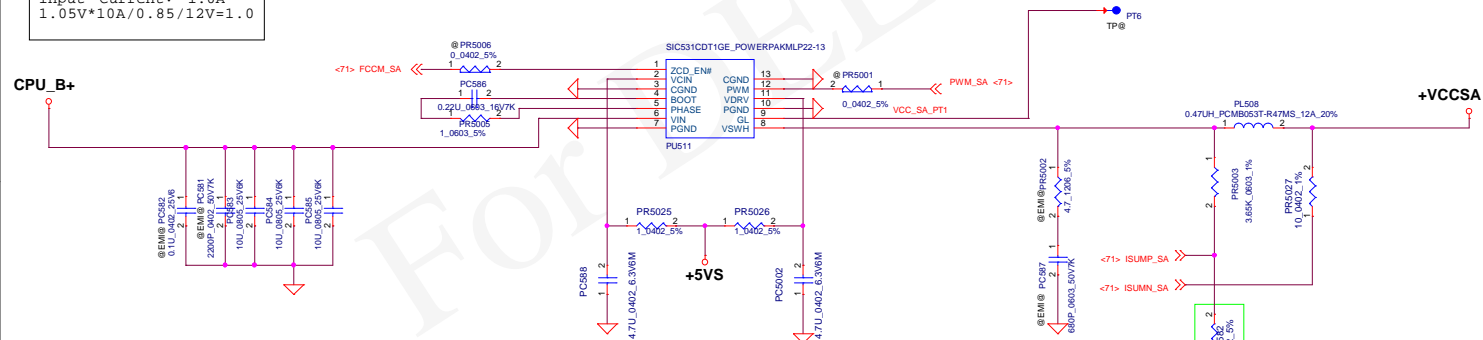
Rev 0.1
 Date: Wednesday, 10/22/2015 Enst 72 of 76



VCC_SA
TDC PL2 :10A
Peak Current 11A
OCP Current 13.2A
DCR 7.4mohm typ
Load Line 9.1mV/A



Input Current: 1.0A
 $1.05V \cdot 10A / 0.85 / 12V = 1.0$



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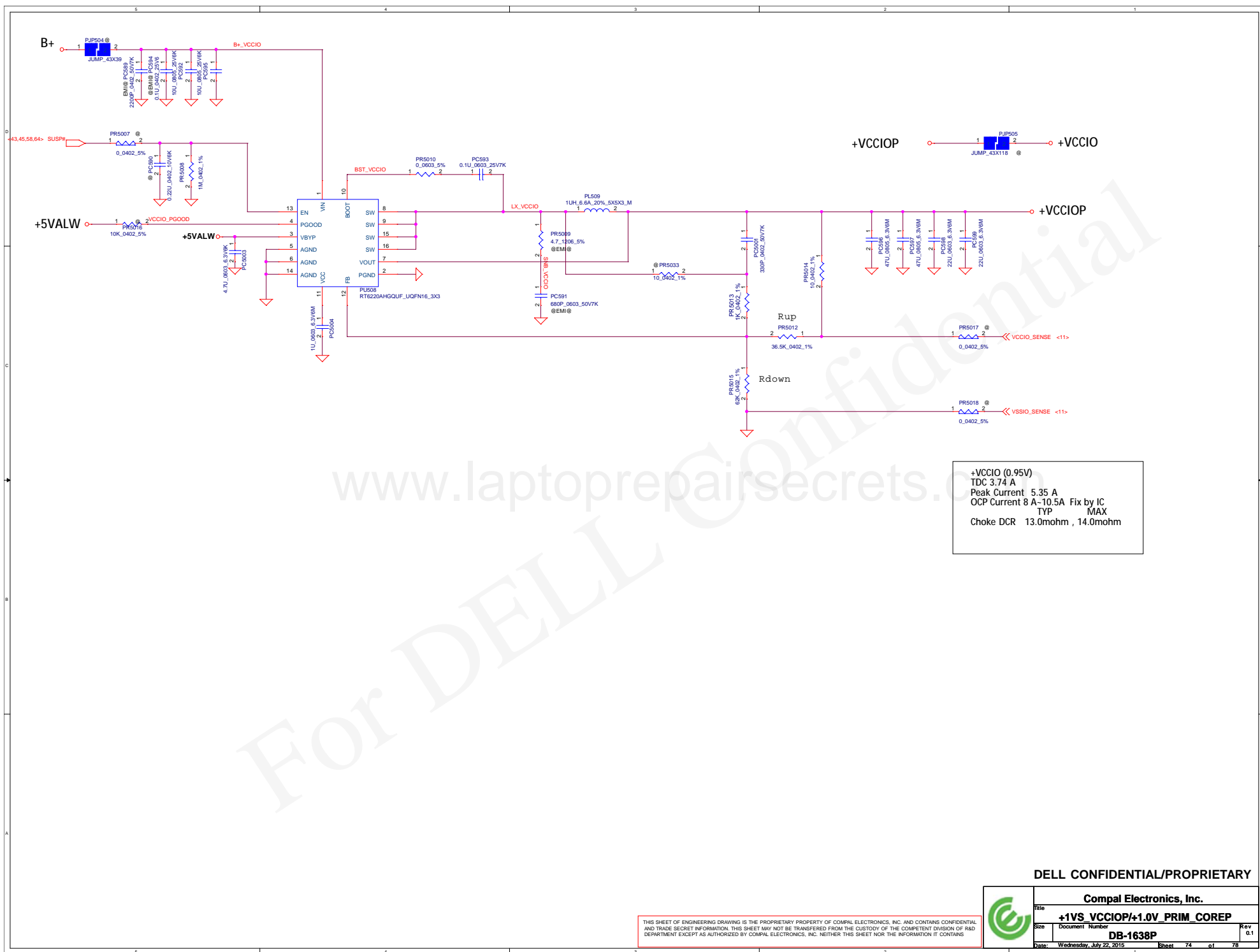
Compal Electronics, Inc.

PWR_VCORE_VGT,VSA

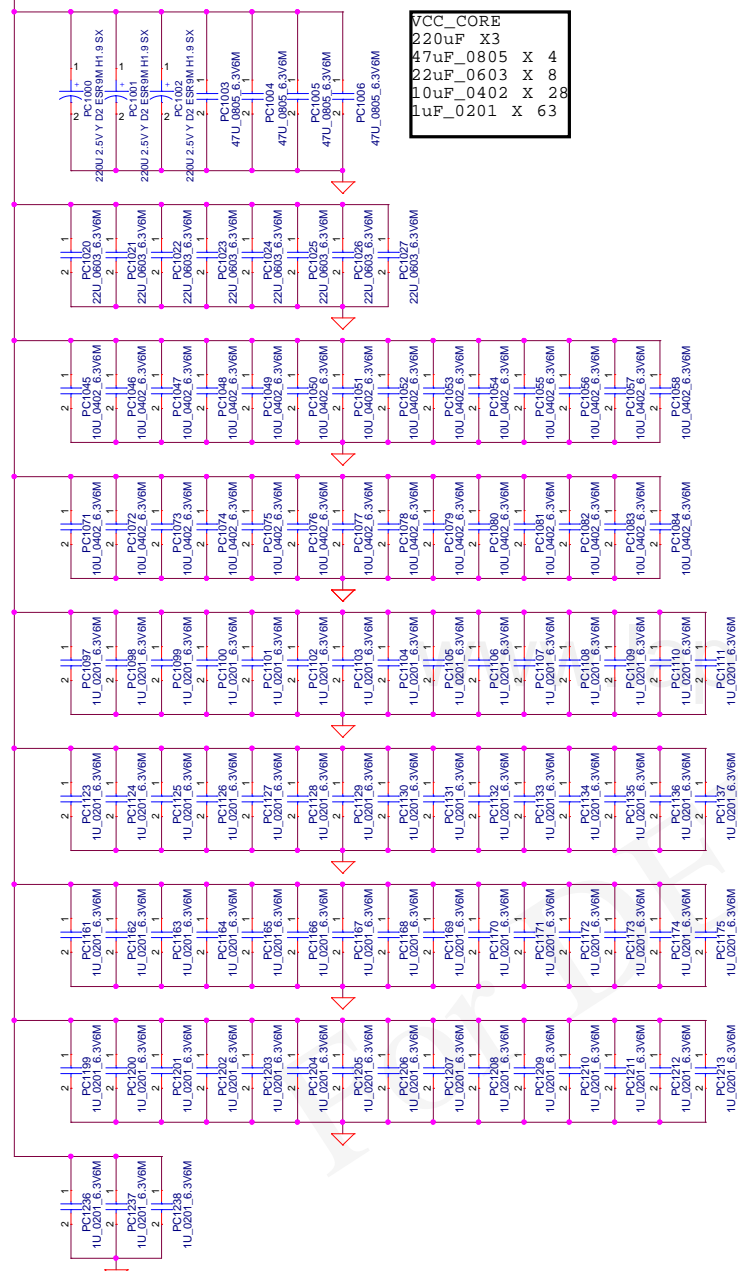
Number
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Rev	01
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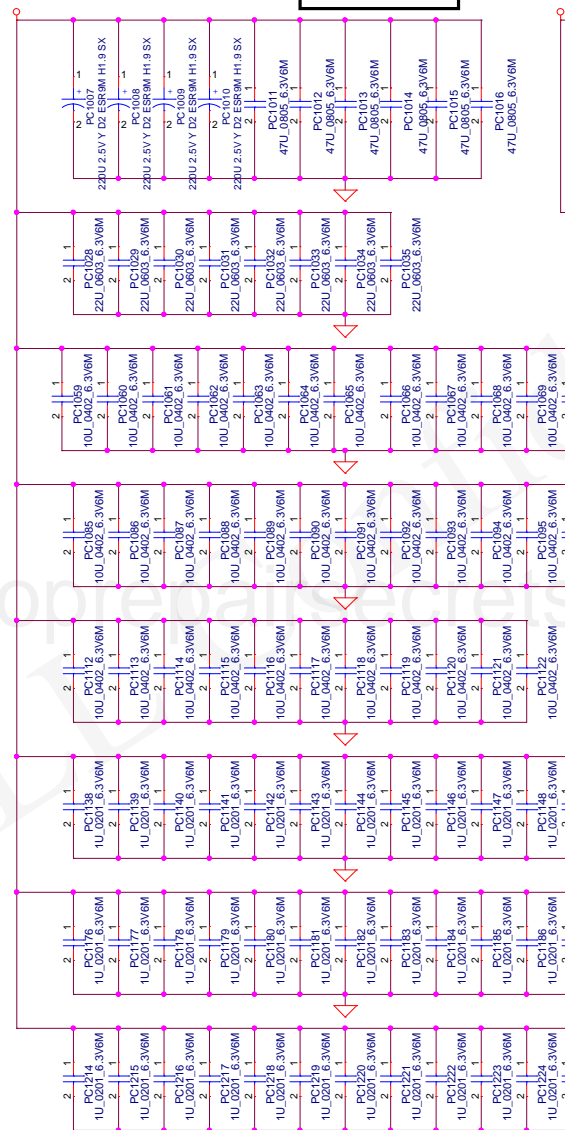
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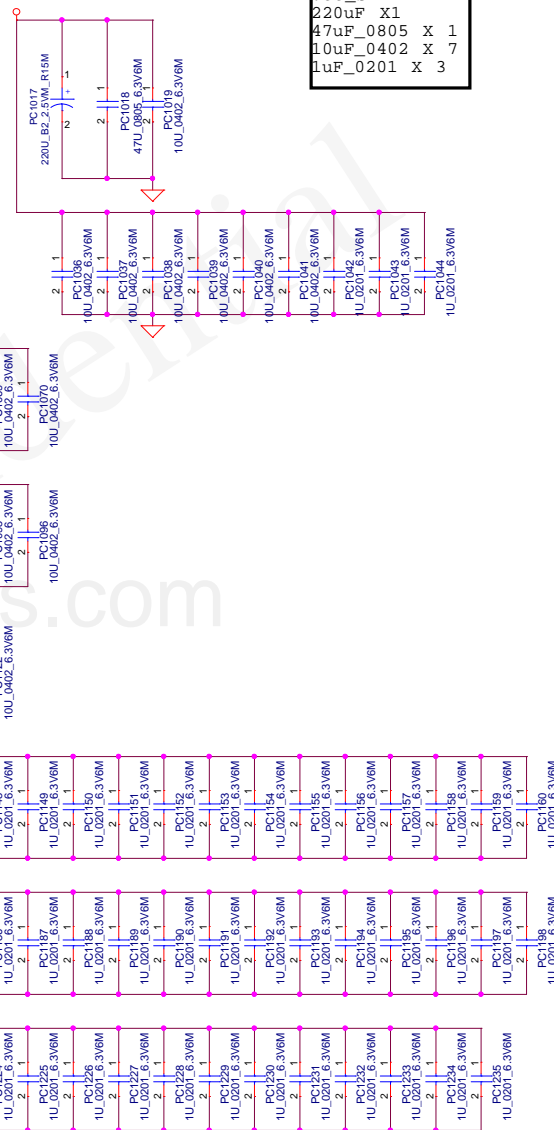
+VCC_CORE



+VCCGT



+VCCSA



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PROCESSOR DECOUPLING

LA-C911P

Size

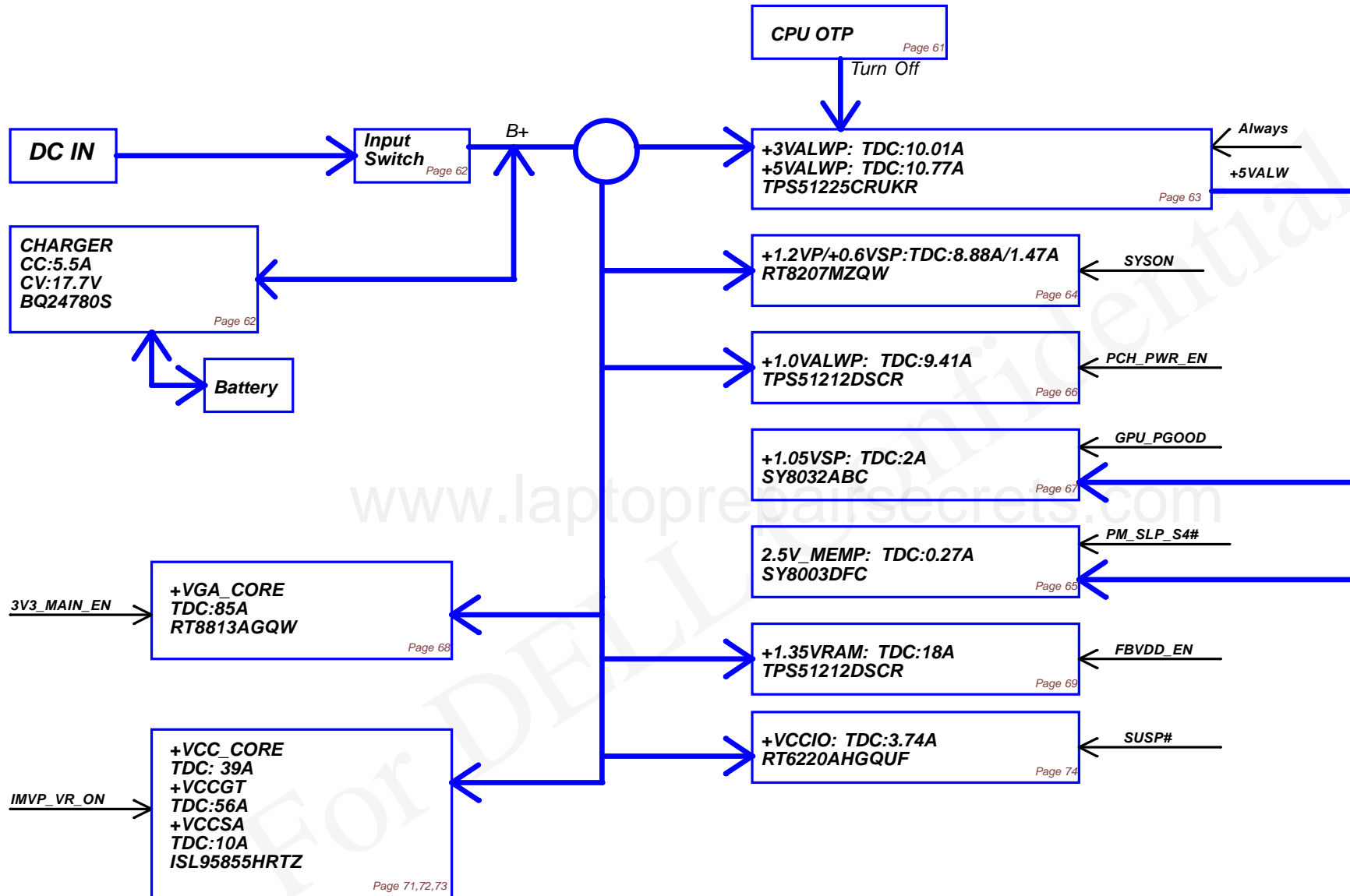
Document Number

Rev 0.1

Date: Wednesday, July 22, 2015

Sheet 75 of 78

Power block



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Title
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				Size Document Number
				LA-C912P
				Rev 0.1
				Date: Wednesday, July 22, 2015
				Sheet 76 of 78

Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	68	PWR_+VGA_CORE	2015.4.1	Nick_Lin	Change VGA_CORE Choke	Change from S COIL .12UH 20% PCME063T-R12MS0R625 41A (SH00000QR00) to 0.15UH_PCME064T-R15MS0R667_36A_20% (SH00000U300) Location:PL600,PL601,PL602	
2	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	Change net from +1.0V_VCCST to +VCCST		
3	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	umount PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	Change from100_0402_1% (SD034100080) to @ Location:PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	
4	66	PWR_+1VALWP	2015.4.11	Nick_Lin	Change OCP setting	Change from 210K_0402_1%_0402_1% (SD034210380) to 86.6K_0402_1% (SD034866280) Location:PR303	
5	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Mount PC627 for Acoustic	Change from 10U_0805_25V (SE00000QK00) to 22U_0805_25V (SE00000XH80) Location:PC638	
6	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Change PC630 for Acoustic	Add 22U_0805_25V (SE00000XH80) Location:PC627,PC630	
7	62	PWR_CHARGER	2015.4.11	Nick_Lin	Change PR702 for PMON function	Change from 0.004_1206_1% (SD000017Q00) to 0.005_1206_1%(SD000017R00) Location:PR303	
8	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form SD000009480 (S RES 1/16W 1.47K +-1% 0402) to SD034127180 (S RES 1/16W 1.27K +-1% 0402) Location PR524 Change form SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000UUV00 (S RES 1/16W 3.6K +-1% 0402) Location PR530 Change form SE068221J80 (S CER CAP 220P 25V J NPO 0402) to SE074152K80 (S CER CAP 1500P 50V K X7R 0402) Location PC514 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD000003480 (S RES 1/16W 316 +-1% 0402) Location PR532 Change form SE074681K80 (S CER CAP 680P 50V K X7R 0402) to SE074331K80 (S CER CAP 330P 50V K X7R 0402) Location PC522 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034453180 (S RES 1/16W 4.53K +-1% 0402) Location PR537 Change form SD034113380 (S RES 1/16W 113K +-1% 0402) to SD034110380 (S RES 1/16W 110K +-1% 0402) Location PR539 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE076333K80 (S CER CAP .033U 16V K X7R 0402) Location PC530 Change form SD034267080 (S RES 1/16W 267 +-1% 0402) to SD034301080 (S RES 1/16W 301 +-1% 0402) Location PR541 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC533	

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					LA-B751P	0.1
				Date:	Wednesday, July 22, 2015	Sheet 77 of 78

Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
9	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form 'SD034100180 (S RES 1/16W 1K +-1% 0402) to 'SD034487100 (S RES 1/16W 4.87K +-1% 0402) Location 'PR511 Change form 'SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to 'SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402) Location 'PC517 Change form 'SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to 'SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location 'PC508 Change form 'SD034182180 (S RES 1/16W 1.82K +-1% 0402) to 'SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location 'PR521 Change form 'SD034953280 (S RES 1/16W 95.3K +-1% 0402) to 'SD034976280 (S RES 1/16W 97.6K +-1% 0402) Location 'PR500	
10	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VCC_CORE VR_IMAX	Change form 'SD034301080 (S RES 1/16W 301 +-1% 0402) to 'SD034442080 (S RES 1/16W 442 +-1% 0402) Location 'PR541 Change form 'SD034243180 (S RES 1/16W 2.43K +-1% 0402) to 'SD034357180 (S RES 1/16W 3.57K +-1% 0402) Location 'PR550 Change form 'SD034562180 (S RES 1/16W 5.62K +-1% 0402) to 'SD034280280 (S RES 1/16W 28K +-1% 0402) Location 'PR517 Change form 'SD034931280 (S RES 1/16W 93.1K +-1% 0402) to 'SD034953280 (S RES 1/16W 95.3K +-1% 0402) Location 'PR548	
11	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VR_ProcHOT Trig point	Change form 'SD034105280 (S RES 1/16W 10.5K +-1% 0402) to 'SD00000AJ80 (S RES 1/16W 12.4K +-1% 0402) Location 'PR545, 'PR514	
12	61	PWR_DCIN / BATT CONN / OTP	2015.6.24	Nick_Lin	fine tune OTP setting	Change form 'SD034162280 (S RES 1/16W 16.2K +-1% 0402) to 'SD034147280 (S RES 1/16W 14.7K +-1% 0402) Location 'PR24	

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					LA-B751P
				Date:	Wednesday, July 22, 2015
				Sheet	78 of 78
				Rev	0.1